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SATURN INTEGRATED CIRCUIT
RELIABILITY TEST PROGRAM

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SECTION I

1.0 INTRODUCTION

This is the Second Quarterly Report on the work performed under Contract NAS8-18018 "SATURN Integrated Circuit Test Program" which is being performed for NASA, George C. Marshall Space Flight Center, Huntsville, Alabama.

The goal of this program is to investigate the reliability characteristics of integrated circuits so that the dominant failure modes and mechanisms can be identified and effective screening tests developed for the devices studied in this program. The test sample in this program represents three basic manufacturing processes. One device type, the MC-1519, contains one compatible thin film die and one monolithic transistor die. The other devices (e.g. the MC-1525, MC-1530, and SN-526A) are the single die all-diffused monolithic structure. Functionally, the MC-1510 and the MC-1525 represent a class of differential amplifiers, while the MC-1530 and SN-526A represent a class of operational amplifiers; and in the case of the SN-526A, possible use as a high gain differential amplifier. The SN-526A was procured from Texas Instruments, Inc. These particular circuits were chosen as being representative of the single types of processes which may be used to manufacture integrated linear circuits.

This report adds to the First Quarterly Report. It includes a description of the electrical parameter measurements for the MC-1530, SN-526A, and the MC-1525 and the life test circuit analysis for the MC-1530 and the MC-1525 circuits. In addition, the test program description is repeated and updated to include progress obtained as of January 1, 1967. Finally, the results of a reliability data survey are included.

SECTION II

2.0 TEST DEVICES

2.1 Description of Test Devices

Four different integrated circuit amplifiers have been selected for this program. The three circuits manufactured by the Motorola Semiconductor Products Division are the MC-1519, MC-1525, and MC-1530. That manufactured by Texas Instruments, Inc. is the SN-526A. These circuits differ among themselves in their performance characteristics, manufacturing processes and methods of packaging (Table 2-1).

TABLE 2-1
COMPARISON OF TEST DEVICES

DEVICE TYPE	TYPE OF AMPLIFIER	MANUFACTURING PROCESS	TYPE OF PACKAGE
MC-1519	Differential	Monolithic P-N-P and Monolithic N-P-N w/thin Film Resistors	10-lead TO-5 Package
MC-1525	Differential	Monolithic w/diffused Resistors	10-lead TO-5 Package
MC-1530	Operational	Monolithic w/diffused Resistors	10-lead alumina Flat Package (1/4" x 1/4")
SN-526A	Operational	Monolithic w/diffused Resistors	10-lead welded Flat Package (1/4" x 1/8")

A more detailed description of these circuits can be found in the First Quarterly Report.

SECTION III

3.0 ELECTRICAL CHARACTERISTICS

The parameter characteristics of these integrated circuits are discussed in this report. As will be seen, the measurement definitions are similar for most circuits. The differences of importance are those techniques used to make the measurements. The discussion presented in this section will compare the parameters at each circuit separately, discussing their similarities using tabular and schematic presentations wherever necessary. Distribution analysis will also be included to show the relative distributions in a graphic presentation.

3.1 Special Test Method Requirements by Device

3.1.1 Differential Amplifier - MC-1519

Figure 3-1 shows the circuit configuration employed in measuring the electrical characteristics of the MC-1519 in the common emitter (CE) mode. This circuit is used in principle, for fixing the circuit current for all measurements. An operational amplifier circuit provides the constant current flow through the input stage required in all test measurements. In the measuring circuits described herein, the amplifier symbol \triangleright is used to designate the circuit as shown in Figure 3-1 with the operational amplifier modification.

3.1.2 SN-526A, MC-1530, MC-1519

In describing the measuring circuits used for these circuits, the amplifier symbol \triangleright will be defined as the integrated circuit device under test. For those circuits and tests requiring roll off capacitors for stabilization, these items are not included in the description of the individual test method.

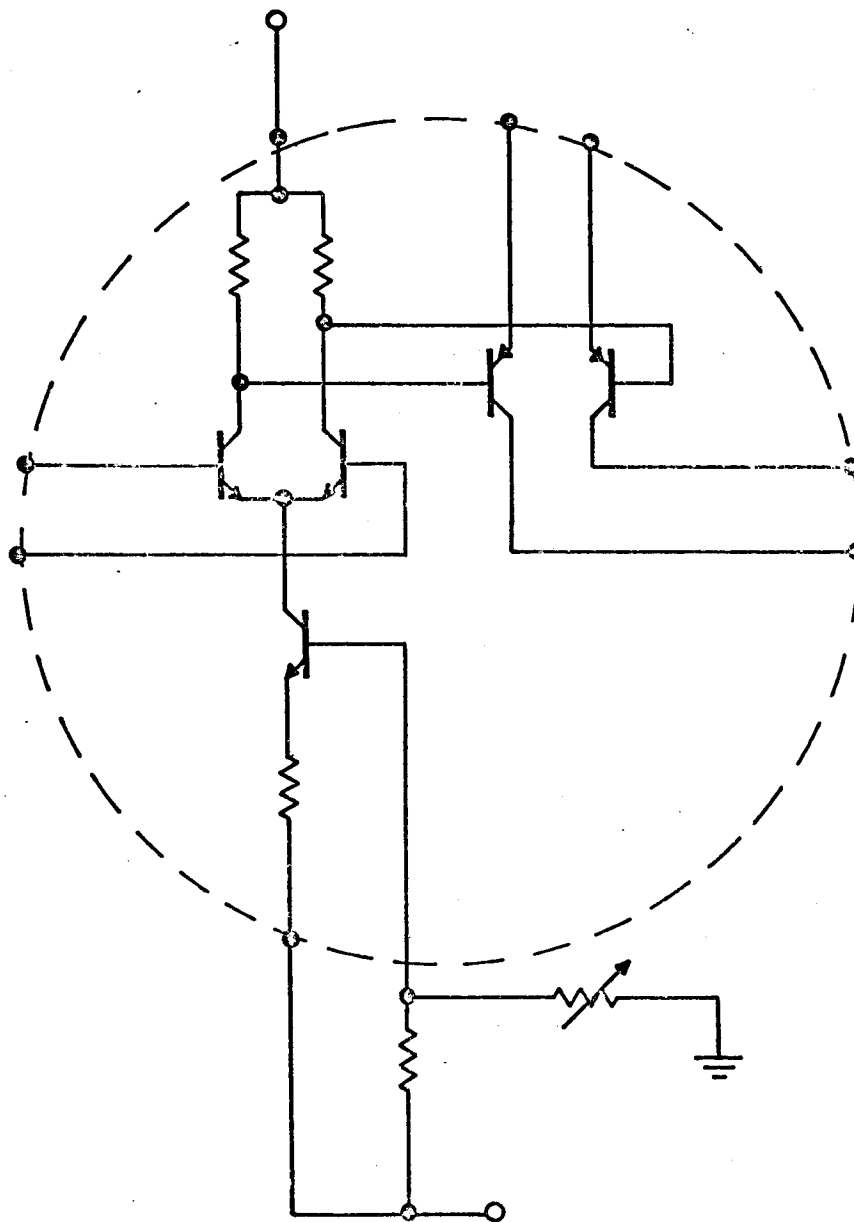


Figure 3-1. Schematic Diagram of MC-1519

3.2 Test Measurement Techniques

3.2.1 Input Offset Voltage (V_{io})

The input offset voltage is defined as the dc voltage which must be applied between the input terminals to obtain zero-differential-output voltage for double ended amplifiers, or zero-output voltage referenced to ground for single ended amplifiers. Without this voltage applied, the amplifier becomes unbalanced and the output voltage level will deviate from ground by an amount equal to the input offset voltage times circuit gain and with the opposite electrical polarity. Each amplifier used in this program has a two-sided input thereby requiring a measurement of the input offset voltage.

The technique used for setting V_{io} is essentially the same for all devices. In one device, the MC-1519, the voltage drop was measured across a resistor divider (1/1000) and divided by 1000 to obtain the actual V_{io} . For the other three circuits, the measurement was taken at the input terminals and read directly on a digital vacuum tube voltmeter. The equivalent circuit is as follows for this measurement.

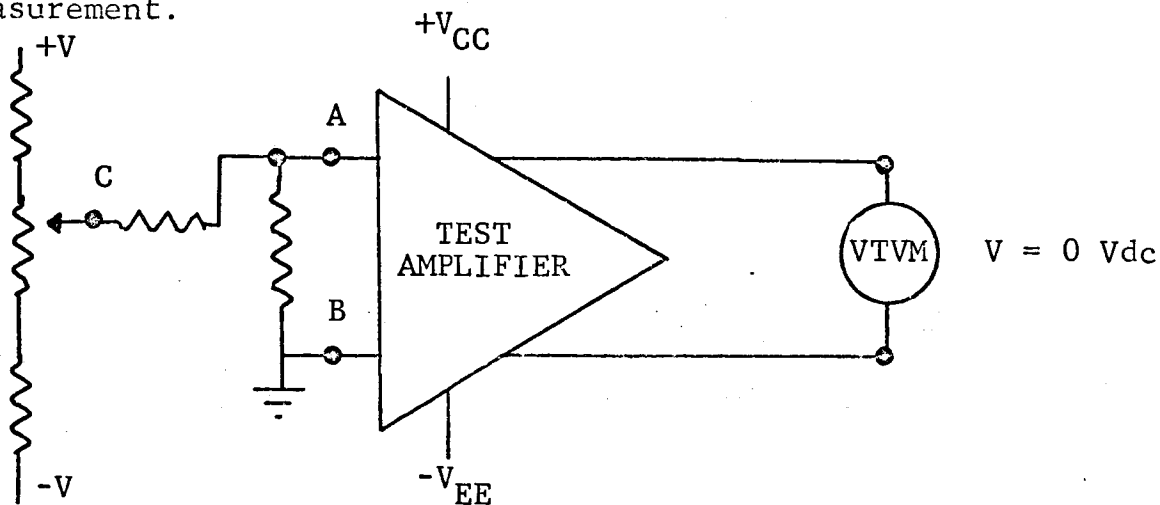


Figure 3-2. V_{io} Test Schematic

V_{io} is measured between points A and B for the MC-1530, MC-1525, and the SN-526A. It is measured between C and B, divided by 1000, for the MC-1519.

3.2.2 Input Current (I_i) and Input Offset Current (I_{io})

For the Motorola circuits, the input current is defined as that current measured at the input when the inputs were connected to the circuit ground through a 100 ohm resistance. That is

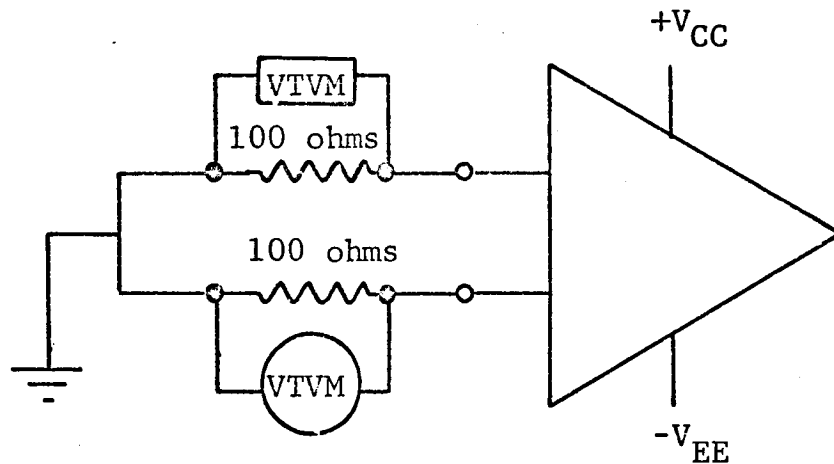


Figure 3-3. I_b and I_{io} Test Schematic

However, the data sheets for the SN-526A circuit calls for the measurement being made when $V_{in} = V_{io}$. To do that, the test method was modified to include the circuit shown for the V_{io} measurement with a current measurement being made in input as a voltage reading through a 10,000 ohm resistance.

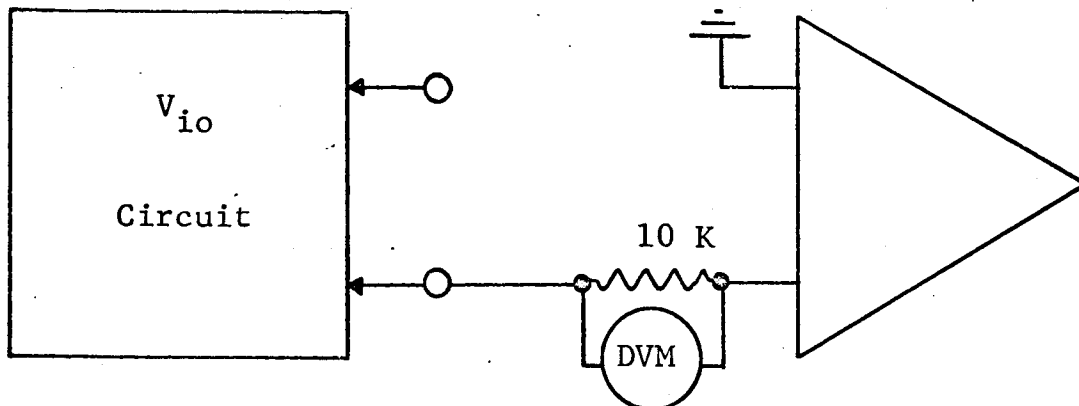


Figure 3-4. SN-526A I_i Test Schematic

Because of the very low input currents, typical values of 50 nA dc, and because the input offset voltage was adjusted at each measurement, the output remained balanced. In designing more rapid measurement techniques, it is assumed that the system designer would take advantage of the high gain operational characteristics of this style of amplifier and utilize a feedback resistor to set V_{io} at the level required to hold the output voltage at approximately 0 volts and then monitor the current in each input lead for the I_{in} measurement.

The differential input current (or input offset current - I_{io}) is defined as the difference in current values for each input and is a computed quantity obtained from the measured input currents. Its significance in this program is that it is a measure of the similarity of the input transistor characteristics and will become important if one of the two input circuits begins to degrade, if its degradation will show up as a function of input circuit.

3.2.3 Differential Voltage Gain (A_{dd})

This measurement is a measure of the circuit's ability to amplify differences in voltages applied to the two input terminals of the differential amplifier. As such, it does not apply to the

single-ended MC-1530 and is used in the measurement of the SN-526A circuit only because it offers both the single-ended and differential amplification characteristics in the same circuit. The measurement required first adjusting the input offset voltage (V_{io}) to the correct value and then applying a small alternating signal across the inputs and measuring the voltage difference at the output terminals under the predetermined load conditions. The differential gain is then defined as the ratio of the output signal to the input signal and can be converted to decibels if desired.

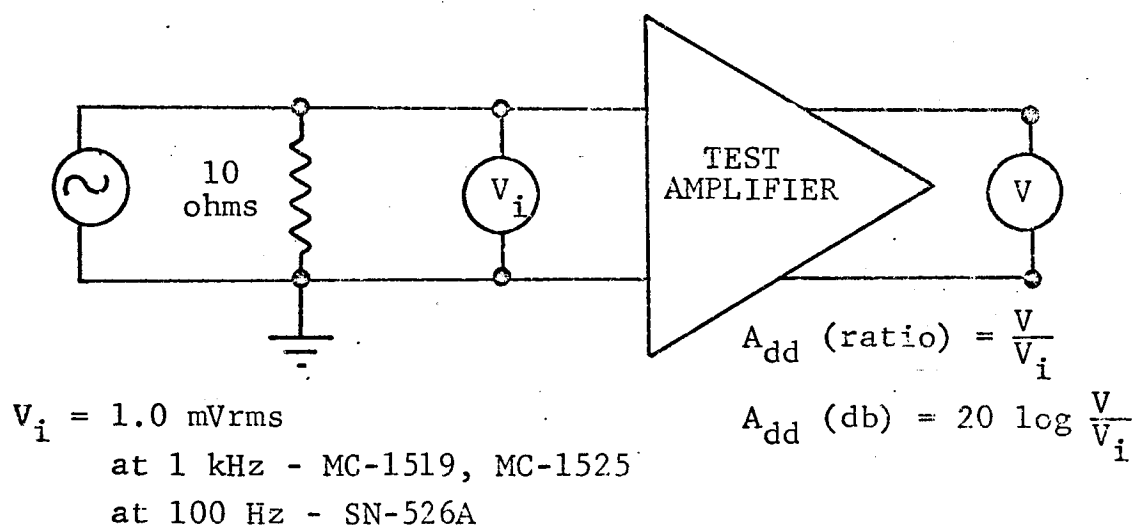
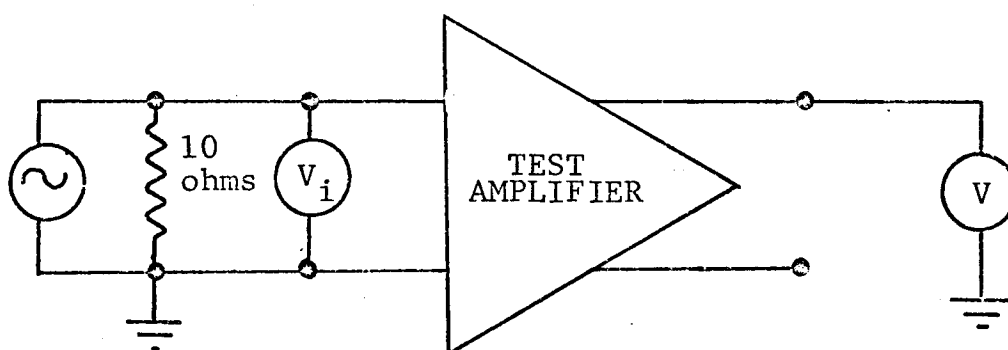


Figure 3-5. Differential Voltage Gain Test Schematic

3.2.4 Single Ended Voltage Gain (A_v , A_{Vol})

The procedure followed in this measurement is similar to that employed in the A_{dd} measurement (Paragraph 3.2.3) except that the output signal is now referenced to ground for one of the halves of the differential amplifier sections and the gain measurement pertains to that part of the amplifier (A_v). For the operational amplifiers, it now becomes a measure of the open loop gain of the

circuit ($A_{V_{01}}$). The significant variations in test procedure for these circuits are the input signal voltage and the oscillator frequency. The gain of the MC-1530 required that the input signal be reduced to 0.1 mV rms to permit undistorted sine waves at the output voltage. All other devices were measured with the input voltage equal to 1.0 mV rms. The Texas Instrument circuit (SN-526A) was measured at a frequency of 100 Hertz because it was specified to be done so. Motorola's circuits were tested at the frequency of 1000 Hertz for the same reason. The circuit measurement technique is generally described as follows:



$$A_V \text{ (ratio)} = \frac{V}{V_i}$$

$$A_V \text{ (db)} = 20 \log \frac{V}{V_i}$$

Figure 3-6. Single Ended Voltage Gain Test Schematic

3.2.5 Maximum Output Voltage Swing (V_o)

In this measurement, the input voltage was increased until the output voltage sine wave begins to become distorted. At this time, the peak to peak voltage is recorded. The significance of this measurement is probably found in its ability to detect leakage in the transistors in the output stages of the amplifier. However, the significance of this measurement remains to be proven, and, for that reason, is not considered a major parameter in this program. Again the oscillator frequency is set according to the published data sheet requirements of each vendor. The test circuit is identical to that used in measuring the single ended gain (A_v and A_{Vol}) except that the input signal is increased until the output distortion occurs.

3.2.6 Bandwidth (BW), Input Impedance (Z_{in}), and Common Mode Rejection (CM_{Rej})

These parameters are the ones which require considerable time for each parameter measurement, while being less significant as reliability study test parameters. Therefore, they are being made on those samples being life tested, both operational and storage, initially, at 1000 hours, and at each 1000 hour readout thereafter. The measurement techniques being used for some tests differ appreciably from those published in the applicable brochures. For instance, the ac input resistance measurement assumes the idealistic relationship that when $R_{in} = Z_{in}$, then V_o will be reduced by a factor of 2 resulting in a 6 db drop in output signal. In each instance, however, it is necessary to adjust V_{io} to balance the output

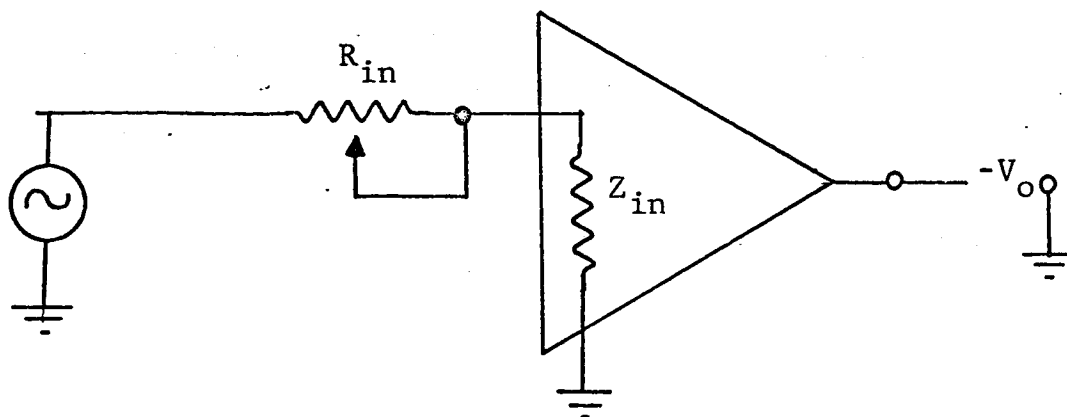


Figure 3-7. Input Impedance Test Schematic

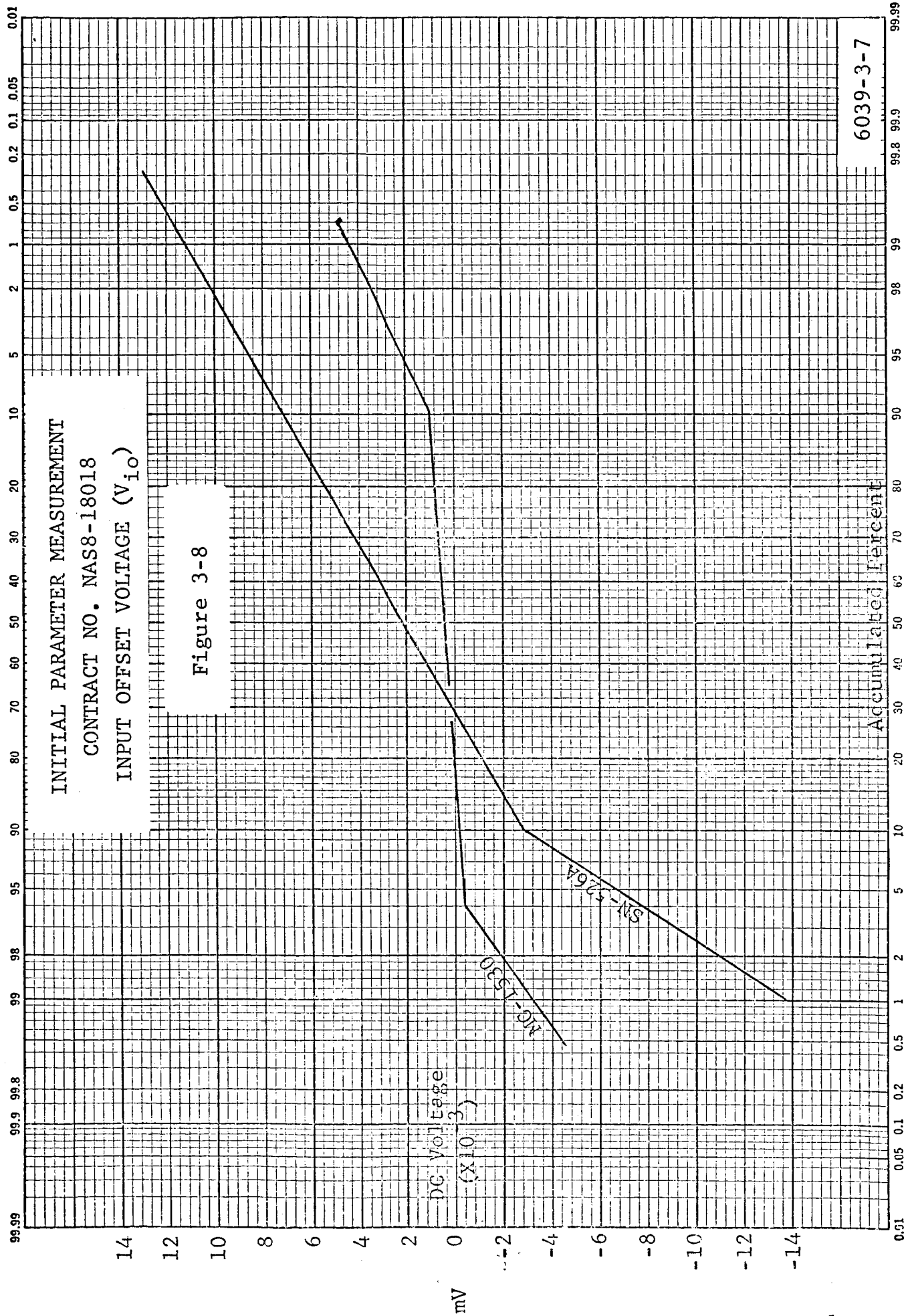
voltage. As is illustrated in Figures 3-9 and 3-10, the value of the dc input current is too large to permit such a simple circuit to be workable. When problems of this nature existed, modifications to procedures were incorporated that permitted the measurement to be made.

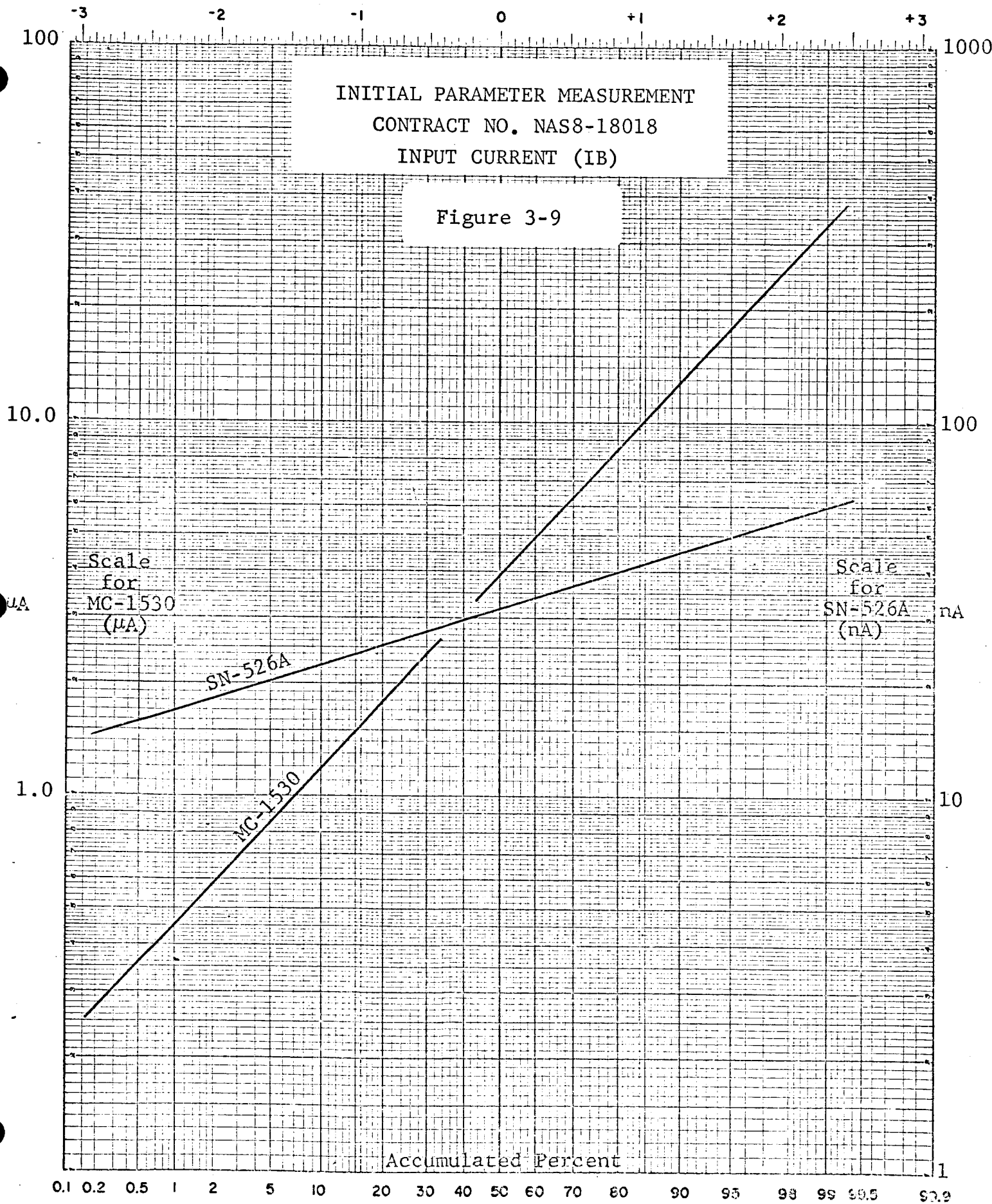
3.3 Program Test Parameters

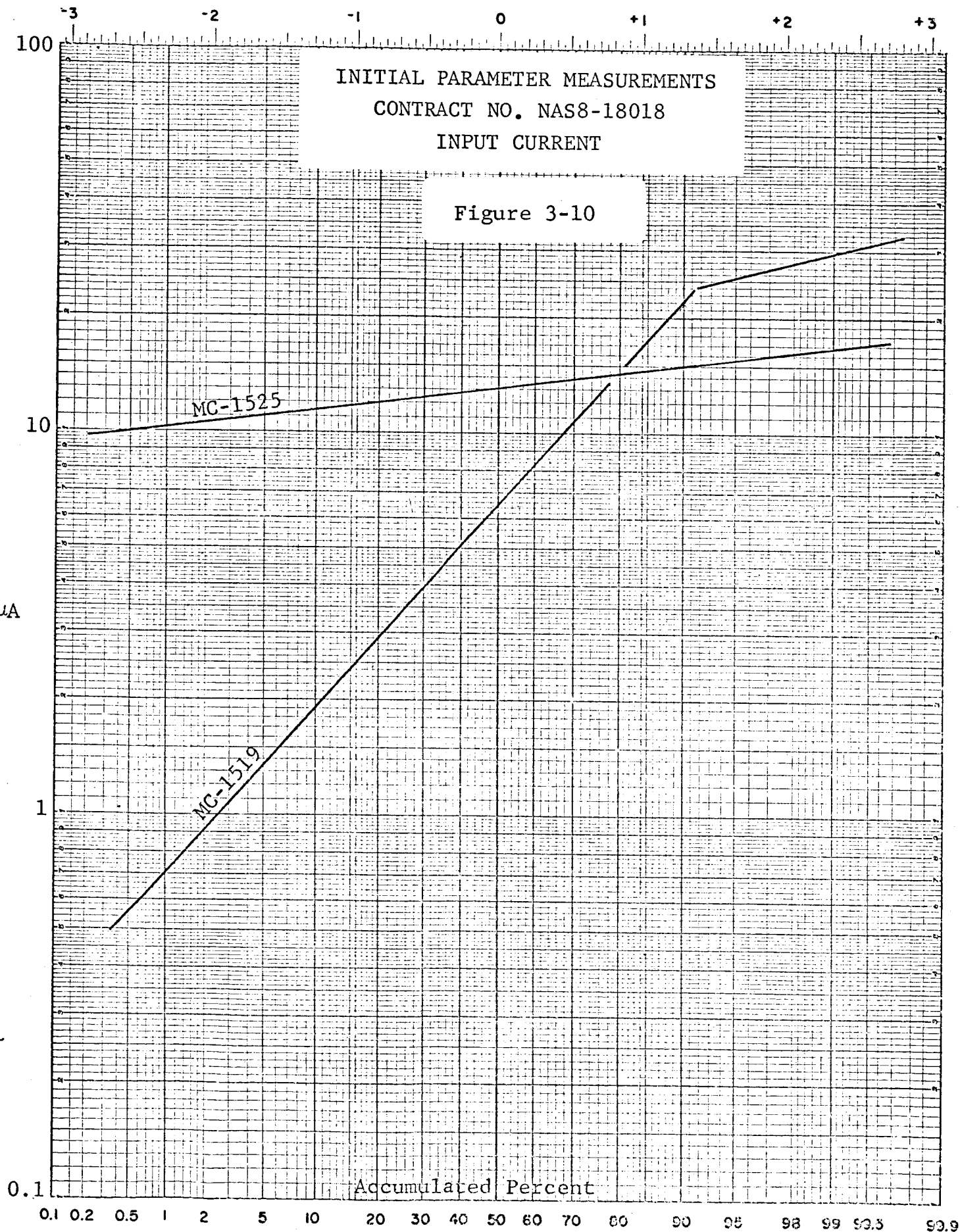
A summary of the test parameters measured, their limits, and the actually recorded values are summarized in this section. The normal distribution graphs are representative of total test sample. The limits selected for the SN-526A have been arbitrarily selected by the test program personnel, based on distribution data shown here, for in none of the published documents available for this circuit is there a list of minimum or maximum limits. This is not a critical problem for the final data analysis will include an evaluation of parameter degradation as a result of applied stresses. All measurements recorded in this section are performed at room temperature (approximately 25°C).

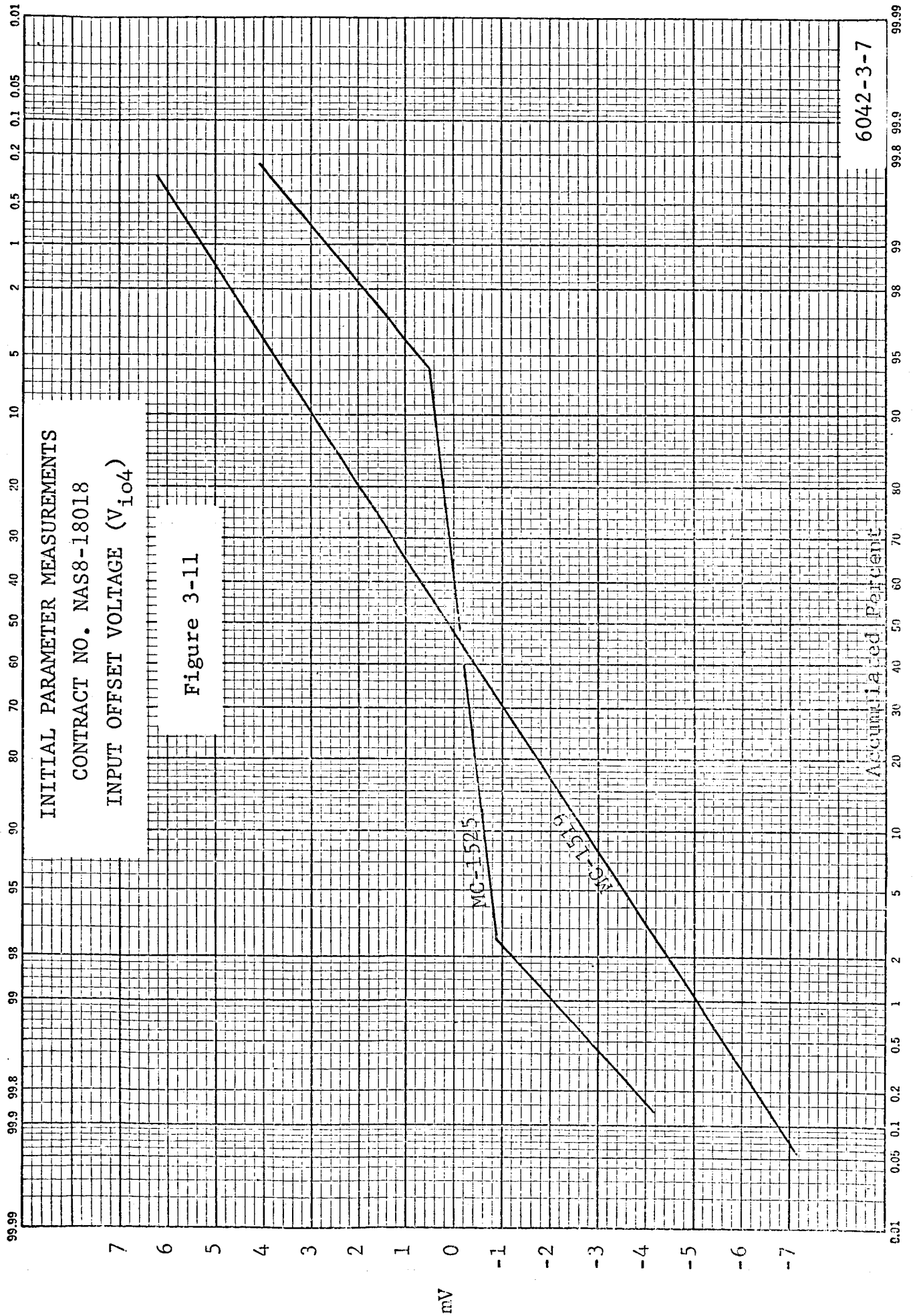
3.3.1 Table of Test Parameters

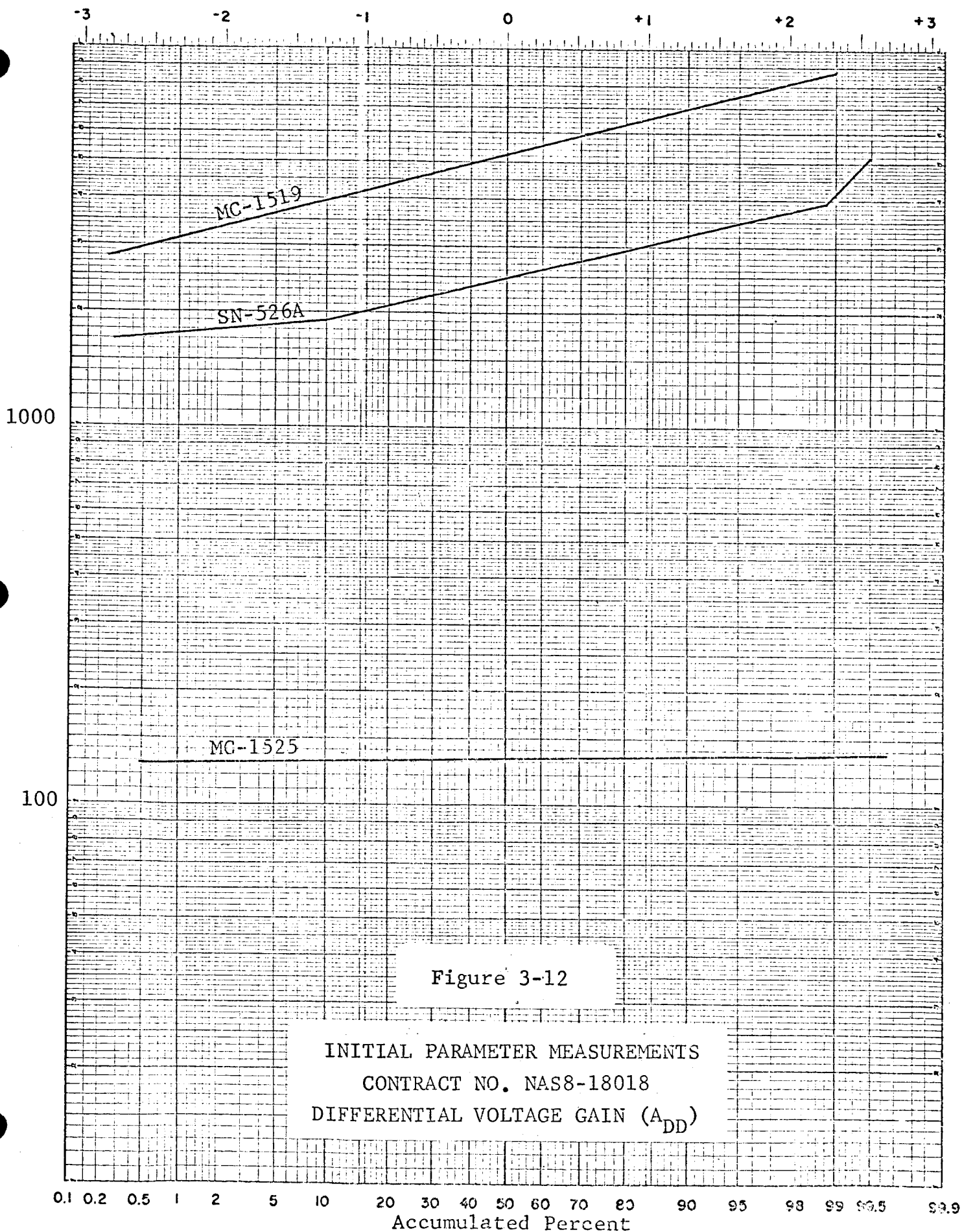
A list of the test parameters and their initial limits is found in Table 3-1. The endpoint limits are found in Tables 3-2, 3-3, 3-4, and 3-5.

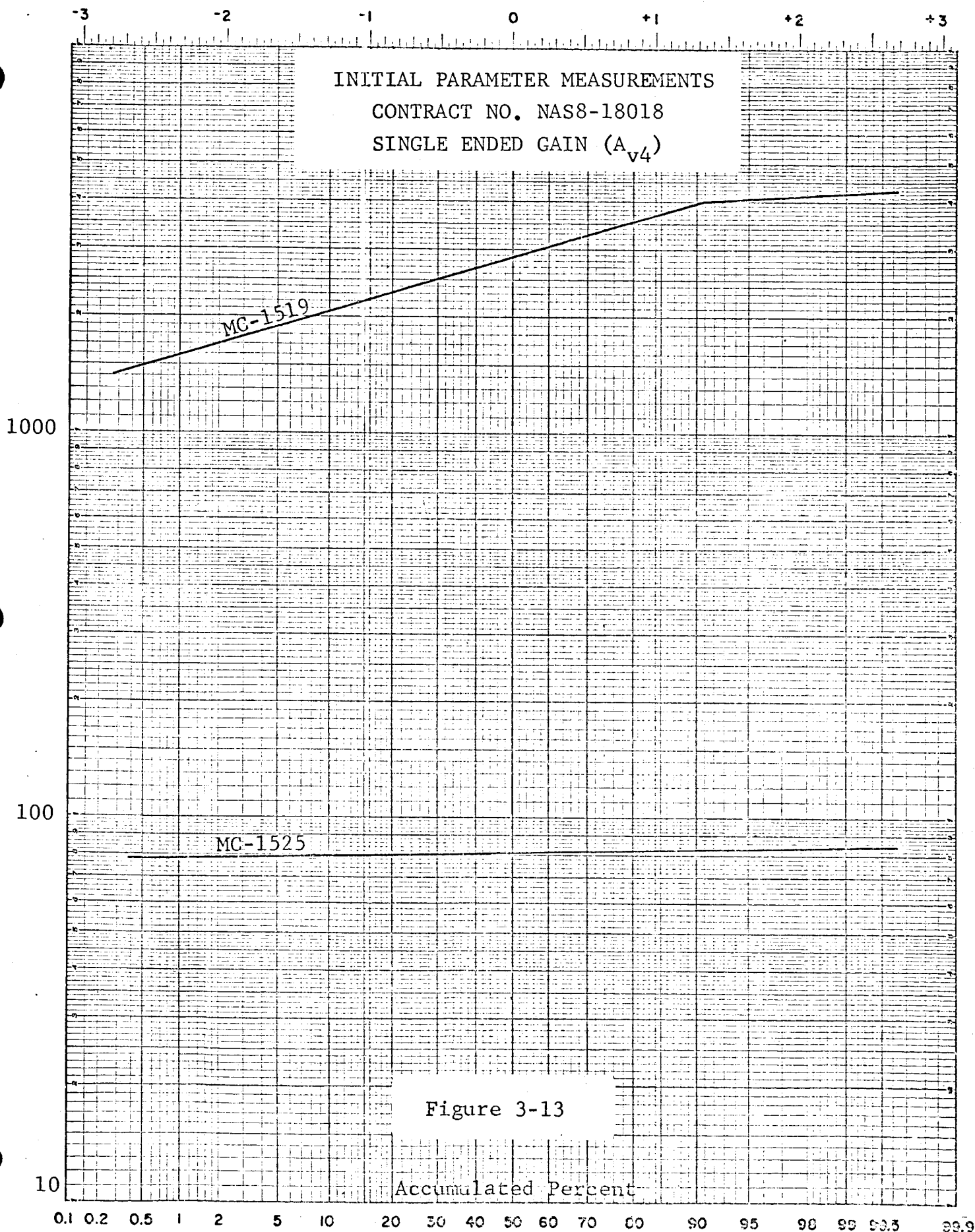


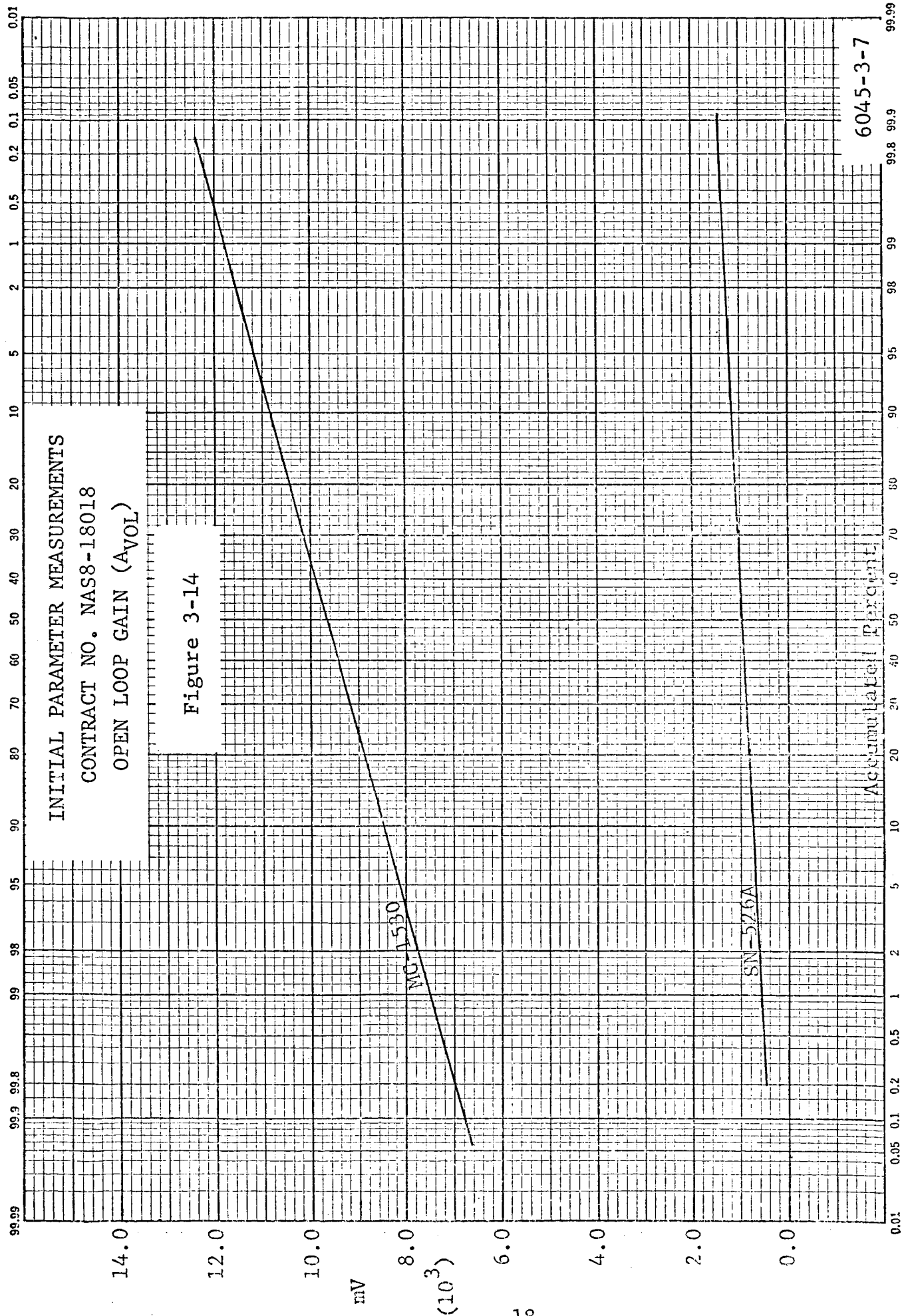


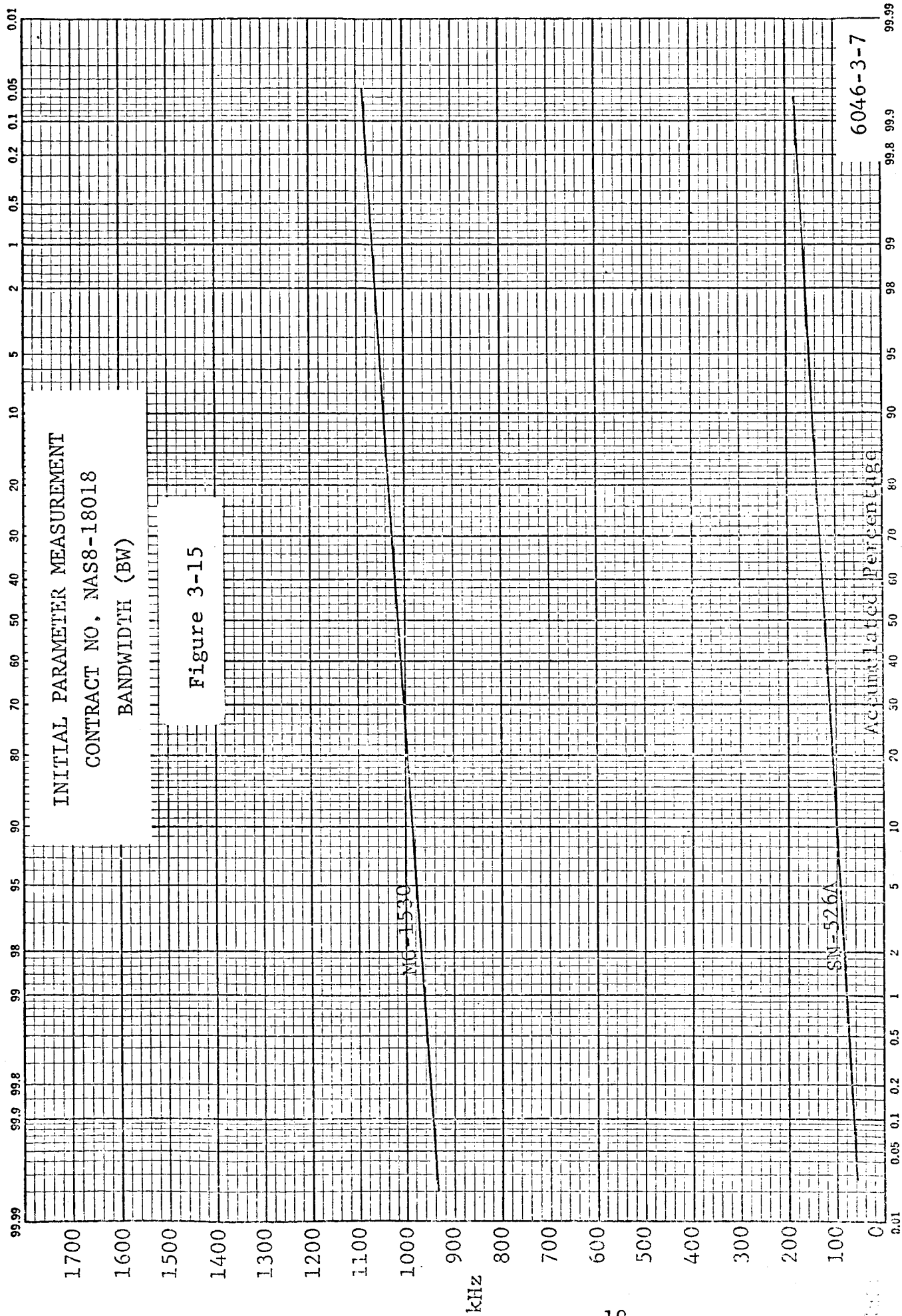


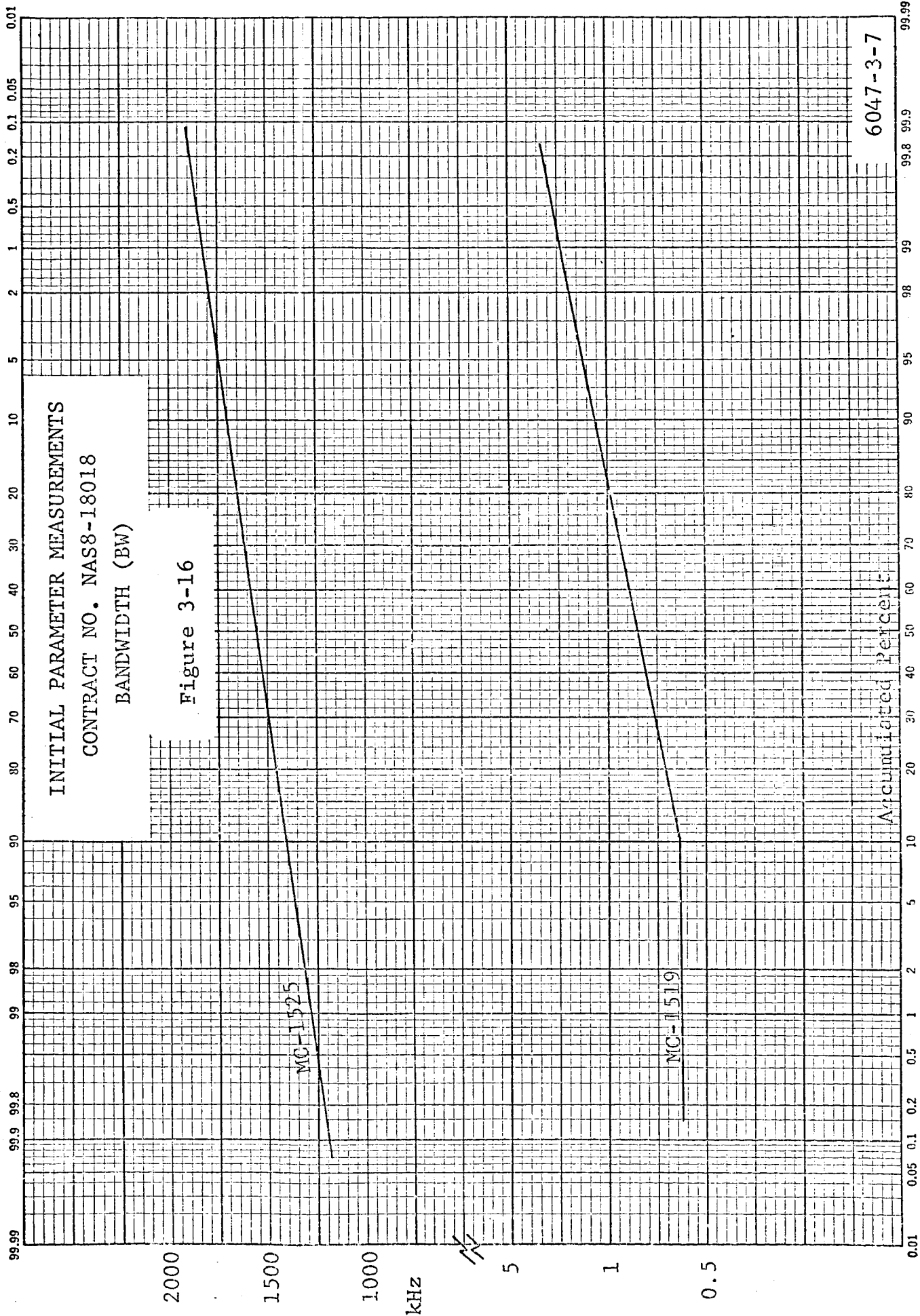












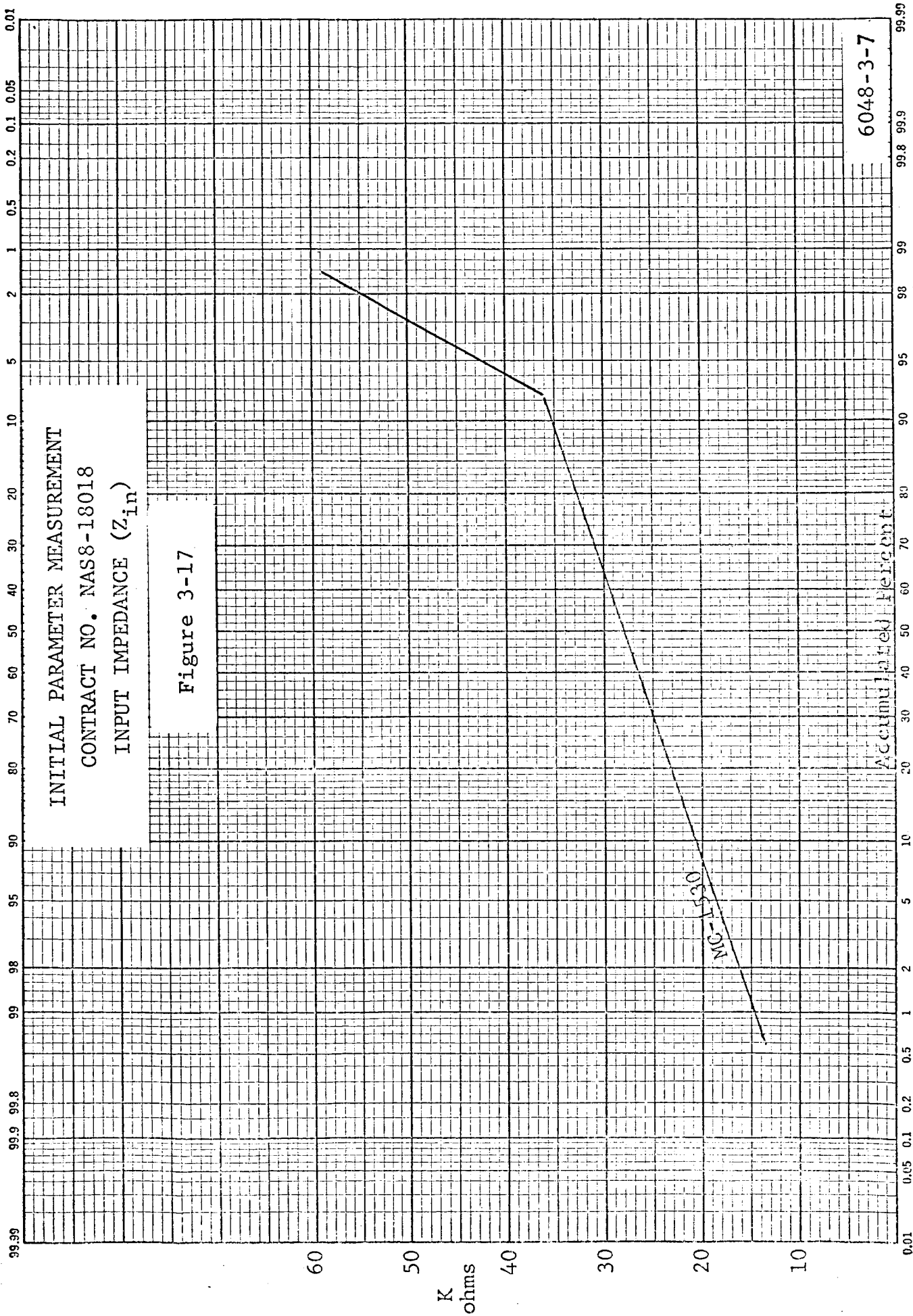


TABLE 3-1
INITIAL LIMITS OF TEST PARAMETERS

MC-1519		MC-1530		SN-526A		MC-1525	
Parameter	Initial Limits	Parameter	Initial Limits	Parameter	Initial Limits	Parameter	Initial Limits
A_{v4}	1.4-5.52 V	I_{B1}^*	10 uA	I_{B7}^*	0.5 uA Max.	A_{dd}	120-160 V
V_{io8}	6.0 mV Max.	I_{B2}^*	10 uA	I_{B8}^*	0.5 uA Max.	$V_o(CM)^*$	6.0-8.0 V
V_{io4}	6.0 mV Max.	I_{io}^*	2 uA	V_{io8}	± 20 mV	V_o	7.0 V Min.
V_o	12.0 V Min	V_{io}	5 mV Max.	V_{io7}	± 20 mV	V_{io}	5.0 mV Max.
A_{dd}	2.8-11.03 V	V_o	9.0 V Min.	A_{dd}	2.0-10.0 V	I_{io}^*	4.0 uA Max.
Z_{in}^*	1.8 K ohm Min.	A_{VOL} at $V_{in}=0.1mV$	0.45-1.25 V	A_{VOL}	1.0-5.0 V	I_{in}^*	20 uA Max.
BW*	630 KC Min.	B_{WOL}^*	1 MHz Min.	BW*	50 kHz Min.	CM_{Rej}^*	80 db Min.
I_4^*	0.7-70 uA	V_{ICM}^*	2.0 V Min.	V_o	9.0 V Min.	BW*	1400 db Min.
I_8^*	0.7-70 uA	Z_{in}^*	10 K ohm Min	V_{OL}	5.0 V Min.	Z_{in}^*	2.0 K ohm Min
		CM_{Rej}^*	70 db Min.	Z_{in}	10 M ohm Min		

* Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-2
PRELIMINARY MC-1519 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
A_{v4}	1.4 - 5.52	1.0 - 10.0	Inoperative	Volts
V_{io8}	6.0 Max.	7.0 Max.	10 Max.	mV
V_{io4}	6.0 Max.	7.0 Max.	10 Max.	mV
V_o	12.0 Min.	10 Min.	Inoperative	Volts
A_{dd}	2.8 - 11.03	2.0 - 20	Inoperative	Volts
Z_{in}^*	1.8 Min.	1.6 Min.	Less than 0.5	K ohm
BW^*	630 Min.	Information Parameter		KC
I_4^*	0.7 - 70	0.5 - 100	0.1 - 300	uA
I_8^*	0.7 - 70	0.5 - 100	0.1 - 300	uA
$V_{CM(out)}^*$	Information Parameter			
$V_{CM(in)}^*$	Information Parameter			

* Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-3
PRELIMINARY MC-1530 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
I_{B1}^*	10 μ A	$\pm 20 \mu$ A	$\pm 100 \mu$ A	μ A
I_{B2}^*	10 μ A	$\pm 20 \mu$ A	$\pm 100 \mu$ A	μ A
I_{io}^*	2 μ A	4 μ A	20 μ A	μ A
V_{io}	5 mV Max.	7 mV	50 mV	mV
V_o	9.0 Min.	7.5 Min.	2.0	Volts
A_{VOL} at $V_{in}=0.1$ mV	0.45 - 1.25	0.20 - 3.2	Inoperative	Volts
B_{WOL}^*	1 Min.	Information Parameter		MHz
V_{ICM}^*	2.0 Min.	Information Parameter		Volts
Z_{in}^*	10 Min.	8 K ohms	1 K ohms	K ohm
C_{Mrej}^* defined as $\frac{AVOL}{ACM}$ Computed = $20 \log AVOL \times 10^4 - 20 \log \frac{VICM}{2}$	70 Min.	Information Parameter		db

* Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-4
PRELIMINARY SN-526A FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
I_{B7}^*	0.5 uA Max.	2 uA Max.	20 uA Max.	uA
I_{B8}^*	0.5 uA Max.	2 uA Max.	20 uA Max.	uA
I_{io}^*	Information Parameter			
V_{io8}	± 20	± 25	± 50	mV
V_{io7}	± 20	± 25	± 50	mV
A_{dd}	2.0 - 10.0	1.0 Min.	Inoperative	Volt
A_{VOL}	1.0 - 5.0	0.28 Min.	Inoperative	Volt
BW*	50 Min.	Information Parameter		kHz
V_o	9.0 Min.	7.5 Min.	2.0 Min.	Volt
V_{OL}	5.0 Min.	3.5 Min.	1 Min.	Volt
Z_{in}	10 Min.	8	1	M ohm
C_{Mrej}^*	Information Parameter			

* Study parameters. No decisions concerning failure of these circuits are made from these parameters.

TABLE 3-5
PRELIMINARY MC-1525 FAILURE CRITERIA

Parameters	Initial Limits	Final Limits		Units
		Degradation	Catastrophic	
A_{dd}	120 - 160	80 - 200	10 Min.	Volt
A_v				Volt
$V_{o(CM)}^*$	6.0 - 8.0	5.0 - 9.0	-5.0 - +11.5	Vdc
V_o	7.0 Min.	3.5 Min.	1.0 Min.	Volt
V_{io}	5.0 Max.	8.0 Max.	50 Max.	mVdc
I_{io}^*	4.0 Max.	10.0 Max.	40 Max.	uA
I_{in}^*	20 Max.	40 Max.	100 Max.	uA
CM_{Rej}^*	80 Min.	Information Parameter		db
BW^*	1400 Min.	Information Parameter		kc
Z_{in}^*	2.0 Min.	Information Parameter		k ohm

* Study parameters. No decisions concerning failure of these circuits are made from these parameters.

SECTION IV

4.0 TEST PROGRAM

This program is being performed on the four integrated circuit amplifiers described in Section 2. The program includes 200 samples of each type. The tests that these samples will be subjected to are summarized in Table 4-1. A more detailed explanation of each test procedure is found in the following sections.

4.1 Operating Life Tests

Three operating life tests are listed in Table 4-1. Since each of Motorola's circuits can be operated at many circuit power levels, the specific test circuit for tests 1 and 2 is a nonfunctional test with normal bias applied. Test 2 is considered to be a control sample. Test 3 consists of testing these circuits at the maximum permissible temperature and at an accelerated power level. Each test will be performed for a minimum of 1000 test hours and will be extended to 4000 hours, time permitting. Each device under test is, at regular intervals, removed from the stress test, allowed sufficient time to return to room temperature, and then read electrically for those parameters which are determined to be critical to the proper operation of the device. Regular test intervals are 125, 250, 1000 hours and at each 1000 hours thereafter. Failure analysis will be conducted immediately on verified catastrophic failures (opens and shorts). However, on samples exhibiting abnormal parameter degradation that is less than catastrophic, no failure analysis will be performed until enough readouts are accumulated to verify failure and to define the rate of degradation occurring.

An analysis of critical stresses on the circuit elements in the MC-1519 under the operating life test conditions was included in Section 6 of Quarterly Report No. 1. The MC-1530 and MC-1525 analyses are included in this report and the SN-526A analysis is planned for a future report.

TABLE 4-1
PROGRAM TEST PLAN

TEST STRESSES	DEVICE TYPES			
	MC-1519	MC-1525	MC-1530	SN-526A
	Number of Samples for Each Test			
<u>OPERATING LIFE TESTS</u>				
(1) Elevated Ambient	25	25	25	25
(2) Room Ambient	15	15	15	15
(3) Elevated Ambient Accelerated Power	25	25	25	25
<u>STORAGE</u>	15	15	15	15
<u>STEP STRESS TESTS</u>				
(5) Temperature	15	15	15	15
(6) Power ($T_A = 25^{\circ}\text{C}$)	15	15	15	15
(7) Temperature - Power	15	15	15	15
(8) Temperature Cycling	15	15	15	15
<u>MIL-S-19500 TEST SEQUENCES</u>				
(9) Mechanical	25	25	25	25
(10) Thermal	25	25	25	25
<u>SPECIAL STUDIES</u>	10	10	10	10

4.1.1 Test 1 - 125°C Ambient, 100 mW - Bias Life Test

Each circuit selected for this program has been evaluated electrically to determine its applicability to variable power stress testing. Each circuit can be stressed at power levels greater than normal operational would generally require. This test procedure is designed to determine the life reliability characteristics for each circuit at a minimum stress level. The test results at the conclusion of this reporting period are summarized in Table 4-2.

TABLE 4-2
OPERATING LIFE TEST
 $T_A = 125^\circ\text{C}$, $P_d = 100 \text{ mW}$

	Initial Sample Size	Number of Failures at Each Readout					
		Test Time - Hours					
		125	250	500	1000		
MC-1519 Differential Amplifier	25	1	0	0			
MC-1530 Operational Amplifier	25	0	0				
SN-526A Operational Amplifier	25	1	0				
MC-1525 Differential Amplifier	25						

4.1.2 Test 2 - 25°C Ambient, 100 mW - Bias Life Test

This test is performed as a control test and the electrical bias conditions are identical to those used in test 1. The test

ambient is maintained at room temperature. The test results at the conclusion of this reporting period are summarized in Table 4-3.

TABLE 4-3
OPERATING LIFE TEST
 $T_A = 25^{\circ}\text{C}$, $P_d = 100 \text{ mW}$

	Initial Sample Size	Number of Failures at Each Readout					
		Test Time - Hours					
		125	250	500	1000		
MC-1519 Differential Amplifier	15	0	0	0			
MC-1530 Operational Amplifier	15	0	0	0			
SN-526A Operational Amplifier	15	0	0				
MC-1525 Differential Amplifier	15						

4.1.3 Test 3 - Elevated Ambient - Accelerated Bias Life Test

The purpose of this test is to accelerate normal failure modes at junction temperatures in excess of the rated conditions for the device. Each circuit is biased at the 300 milliwatt power level (normal power level- $T_A=150^{\circ}\text{C}$ for the MC-1525). The temperature of these tests will be maintained at the chamber temperature of 125°C . The test results at the conclusion of this reporting period are summarized in Table 4-4. The MC-1525 has a critical applied power limitation which does not permit it to be stressed as planned. In place of this test, it is being tested as in 4.1.1 except that the ambient temperature has been changed to 150°C to adjust the average junction temperature an equivalent amount.

TABLE 4-4
OPERATING LIFE TEST
 $T_A = 125^{\circ}\text{C}$, $P_d = 300 \text{ MW}$

	Initial Sample Size	Number of Failures at Each Readout					
		Test Time - Hours					
		125	250	500	1000		
MC-1519 Differential Amplifier	25	0	1	1			
MC-1530 Operational Amplifier	25	2	0				
SN-526A Operational Amplifier	25	0	0				
MC-1525 Differential Amplifier	25						

4.1.4 Test 4 - Storage Life Test

This test is performed at the ambient temperature of 150°C . It consists of placing the devices, unbiased, in a test chamber and periodically withdrawing them from the chamber for parameter readings. A minimum of four hours is allowed between the time the device removal from temperature stress to the time the test sample's electrical parameters are read. The test results at the conclusion of this reporting period are summarized in Table 4-5.

TABLE 4-5
STORAGE LIFE TEST
 $T_A = 150^{\circ}\text{C}$, $P_d = 0 \text{ mW}$

	Initial Sample Size	Number of Failures at Each Readout					
		Test Time - Hours					
		125	250	500	1000		
MC-1519 Differential Amplifier	15	0	0	0			
MC-1530 Operational Amplifier	15	0	0	0			
SN-526A Operational Amplifier	15	0	0				
MC-1525 Differential Amplifier	15						

4.2 Step Stress Tests

Step stress testing is a technique utilizing small samples, subjected to successively increasing levels of stress, to obtain a maximum amount of reliability information in a relatively short period of time. The testing stress usually used in evaluations of this nature will be any combination of temperature or power or voltage. The technique is not restricted to these methods of testing and is often applied to mechanical tests as well. Intermediate readings are taken after each step.

4.2.1 Test 5 - Temperature Step Stress Test

The devices to be stressed in this manner are stored at each stress temperature for 48 hours. The initial step is set at 150°C for the TO-5 package circuits and 200°C for the flat package circuits. After each stress, the surviving circuits will be stressed

at a level 25°C higher than the previous step. Each test will be continued until more than 67 percent of the sample has failed. The test results at the conclusion of this reporting period are summarized in Table 4-6.

TABLE 4-6
TEMPERATURE STEP STRESS
TIME AT EACH STRESS "T" = 48 HOURS

	Initial Sample Size	Number of Failures at Each Step								
		Temperature Steps								
		150	175	200	225	250	275	300	325	350
MC-1519 Differential Amplifier	15	0	0	0	0					
MC-1530 Operational Amplifier	15	-	-	0	0					
SN-526A Operational Amplifier	15	-	-	0	1					
MC-1525 Differential Amplifier	15									

4.2.2 Test 6 - Power Step Stress Test

Each circuit is stressed at the room ambient temperature by varying the power dissipated in a controlled manner. The devices are subjected to 48 hours of testing at each stress level. The initial power level is 100 milliwatts and each successive step is increased by 100 milliwatts. The tests continue until either 67 percent of the sample has failed, the equipment limitations have been reached, or the circuit limitations have been reached. All

devices passing at one stress level are subjected to the next programmed stress level. The test results at the conclusion of this reporting period are summarized in Table 4-7.

TABLE 4-7
POWER STEP STRESS TEST
 $T_A = 25^{\circ}\text{C}$, TIME AT EACH STEP = 48 HOURS

	Initial Sample Size	Number of Failures at Each Readout										
		Stress Power Level (Watts)										
		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	
MC-1519	Differential Amplifier	15	0	0	0	0						
MC-1530	Operational Amplifier	15	0	0	0	0	1					
SN-526A	Operational Amplifier	15	0	0	0							

4.2.3 Test 7 - Temperature - Power Step Stress Test

The procedure to be used in this test is identical with that defined for test number 6 except that the ambient temperature will be set at 125°C and that the MC-1525 will be step stressed by increasing the ambient temperature in steps of 25°C to a maximum temperature of 225°C . The test results at the conclusion of this reporting period are summarized in Table 4-8.

TABLE 4-8
POWER STEP STRESS TEST
 $T_A = 125^{\circ}\text{C}$

	Initial Sample Size	Number of Failures at Each Readout										
		Stress Power Level (Watts)										
		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	
MC-1519	Differential Amplifier	15	0	0	0	0						
MC-1530	Operational Amplifier	15	0	0	0	0	0					
SN-526A	Operational Amplifier	15	0	0	0							
MC-1525	Differential Amplifier	30										

4.2.4 Test 8 - Temperature Cycling

Each sample is being subjected to 10 cycles of temperature cycling per the procedure listed in Mil-Std-202C except that the temperature extremes are varied for each step in the program as follows:

Step 1 -55°C to 150°C
 Step 2 -55°C to $+175^{\circ}\text{C}$
 Step 3 -55°C to $+200^{\circ}\text{C}$
 Step 4

to

Step n -55°C to $T_{h(n)}$ when less than 33 percent of the initial sample remains good or until the equipment limit has been reached.

$$T_{h(n)} = [150 + 25(n-1)]^{\circ}\text{C}$$

The test results at the conclusion of this reporting period are summarized in Table 4-9.

TABLE 4-9
TEMPERATURE CYCLING STEP STRESS
10 CYCLES PER STEP (MIL-STD-202C)
LOW TEMPERATURE CONSTANT OF $T_A = -55^{\circ}\text{C}$

	Initial Sample Size	Number of Failures at Each Readout						
		Upper Temperature Stress ($^{\circ}\text{C}$)						
		150	175	200	225	250	275	300
MC-1519 Differential Amplifier	15	0	0	0	0	0		
MC-1530 Operational Amplifier	15	0	0	0	0			
SN-526A Operational Amplifier	15	1	1					
MC-1525 Differential Amplifier								

4.3 MIL-S-19500 Test Sequences

Standard integrated circuits are normally expected to pass the two environmental test sequences listed in Mil-S-19500. To verify that this capability still exists in this product, this sequence of testing is added to the test program. Intermediate readings are taken after each test.

4.3.1 Test 9 - Mechanical Test Sequence

The mechanical test sequences and their detailed procedures are defined in the following paragraphs. The test results at the conclusion of this reporting period are summarized in Table 4-10.

TABLE 4-10
MECHANICAL ENVIRONMENTAL TEST SEQUENCE

	Initial Sample Size	Number of Failures			
		Stress			
		Shock 1500 G	Vib. Fat. 20 G	Vib. Var. Freq. 20 G	Constant Accel. 20,000 G
MC-1519 Differential Amplifier	25	0	1	0	0
MC-1530 Operational Amplifier	25	0	0	0	0
SN-526A Operational Amplifier	25	1			
MC-1525 Differential Amplifier	25				

4.3.1.1 Shock Test

The shock test is intended to determine the suitability of devices for use in electronic equipment that may be subjected to moderately severe shocks, resulting from suddenly applied forces or abrupt changes in motion produced by rough handling, transportation or field operation. The shock test is usually performed by rigidly mounting the device under test in a fixture on a carriage between vertical guide rods. The carriage is raised and dropped. The height from which the carriage is dropped and the nature of the pad upon which it drops determine the shock level and period. This shock test is repeated five times along each of three axes, x_1 , y_1 , z_1 , at a shock level of 1500 "G".

4.3.1.2 Constant Acceleration

The constant acceleration test is an "accelerated" test designed to detect types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. The device under test is mounted in a jig on the periphery of a rotating member. The rotational speed and radius from the devices under test to the rotational axis determine the acceleration level of 20,000 G.

4.3.1.3 Vibration Fatigue

The purpose of this test is to determine the effect of prolonged vibration on the device. The integrated circuit device under test is rigidly mounted on a vibration table, and then subjected to a simple harmonic motion at approximately 60 cps with a constant peak acceleration of 20 G minimum for a period of 32 hours in each of three mutually perpendicular orientations for a total of 96 hours.

4.3.1.4 Vibration Variable Frequency

This test is performed for the purpose of determining the effect on devices of vibration through a constantly varying frequency range. The integrated circuit is rigidly fastened to a vibration platform and then vibrated at a constant peak acceleration of 20 G. The vibration frequency is varied approximately logarithmically between 100 and 2000 cps. The entire frequency range of 100 to 2000 cps and return to 100 cps is traversed in not less than 4 minutes. This cycle is performed four times in each of three mutually perpendicular planes.

4.3.2 Test 10 - Thermal Test Sequence

The thermal test sequence and the individual test procedures are defined in the following paragraphs. The test results at the conclusion of this reporting period are summarized in Table 4-11.

TABLE 4-11
THERMAL ENVIRONMENTAL TEST SEQUENCE

	Initial Sample Size	Number of Failures			
		Stress			
		Solder- ability	Temperature Cycling -65°C to 175°C	Thermal Shock 0°C to 100°C	Moisture Resistance 10 Days
MC-1519 Differential Amplifier	25	0	0	0	0
MC-1530 Operational Amplifier	25	0	0	0	
SN-526A Operational Amplifier	25	0	0		
MC-1525 Differential Amplifier	25				

4.3.2.1 Solderability

This test is designed to determine both the ability of the integrated circuit to withstand the high temperature encountered during soldering and to determine how well the leads are wetted to

solder. The test is performed by dipping the package leads into molten 60-40 lead-tin solder at 230°C to a point 1/6 inch from the body of the package for a period of 10 seconds. The circuits are tested for electrical parameters to determine if the test caused any characteristic changes and then are examined under a microscope to determine if the leads have been adequately coated with solder.

4.3.2.2 Temperature Cycling

The temperature cycling test is conducted to determine the resistance of the integrated circuit to repeated exposure to extremes of high and low temperature. A typical temperature cycling test for integrated circuits consists of 30 minutes at -65°C, 5 minutes at +25°C, 30 minutes at +175°C, 5 minutes at +25°C, and return to -65°C. This high and low temperature sequence is repeated five times.

4.3.2.3 Thermal Shock

This test is similar to temperature cycling, except that the transfer time from the extreme temperature is shorter. This test is often referred to as "glass strain." The standard test for evaluating integrated circuits used 0°C and 100°C as extreme temperature limits. The transfer time must be less than 5 seconds. This test is run for five cycles.

4.3.2.4 Moisture Resistance

The purpose of the moisture resistance test is to evaluate, in an accelerated manner, the resistance of integrated circuits to high humidity and temperature conditions. The test period is 10 days, during which the integrated circuit in a chamber is subjected to temperature cycles between +10°C and +65°C at a relative humidity of between 90 and 98 percent.

These test procedures are described in detail in
Mil-Std-750 -- TEST METHODS FOR SEMICONDUCTOR DEVICES.

4.3.3 Additional Testing

At the completion of these standard tests, the survivors from these samples (tests 9 and 10) will be equally divided into three samples and will be stressed, in steps, as follows:

A. Temperature Cycling Step Stress Test

Using the same time sequences performed in the standard test sequence, referred to in test 9, 10 cycles will be performed at each step, with parameter readings performed after each step, until more than 50 percent of the sample has failed or the equipment limitations have been reached.

1st Step	-55°C to +175°C
2nd Step	-55°C to +200°C
nth Step	-55 to $[175 + 25(n-1)]^{\circ}\text{C}$

B. Shock Step Stress Test

10 shocks in each axis (x_1 , y_1 , z_1) will be performed in stress steps of:

3,000 G	0.2 millisecond
10,000 G	0.2 millisecond

with parameter readings to be made after each step.

C. Vibration Variable Frequency Step Stress Test

The sample will be subjected to increased steps of stresses using the same procedure as outlined to be performed in the variable frequency vibration test stress except that the stress levels at each step will be as follows:

Step 1	30 G
2	50 G
3	70 G
4	80 G
5	90 G
6	100 G

Such parameter readings as are necessary to determine whether the die and leads are intact will be taken after each step in the stress sequence. Complete electrical parameter data will be taken at the beginning and at the end of the program.

4.4 Special Studies

These samples are reserved for studies such as thermal electrical characterization through infrared techniques and other special investigations to be determined jointly by NASA-Huntsville and Motorola.

SECTION V

5.0 LIFE TEST CIRCUITS

The purpose of operating life or burn-in tests is to accelerate those mechanisms which lead to premature failure of a device under normal operating stress or to provide an estimate of the life expectancy of devices during normal operation. Functional tests (i.e. operating the device in a fashion similar to which it will be used in a system) are the most attractive to most circuit designers. As integrated circuits become more complex, however, it is increasingly difficult to increase the electrical stress levels so that the basic mechanism which cause failures will be accelerated without either violating the basic principle of applying integrated circuits, violating the operational or functional design of the circuit, or introducing stress levels in the interior of the device which are so far removed from normal operation that correlation between the accelerated level and the normal operating stress level becomes obscure. Other techniques must, therefore, be developed considering not only the physical reactions or processes which lead to failure but the logistic factors of time and facility costs if economical procurement of high reliability linear integrated circuits is to become a reality. This means that burn-in or life testing techniques must be compatible with standard quality assurance procedures. Past experience with digital integrated circuits has indicated that, in a vast majority of cases, a combination of dc bias and temperature will accelerate most of the failure modes that are present. If we consider that the basic structure of linear integrated circuits and the processing techniques utilized in their fabrication are no different than those used in the production of digital integrated circuits, then it follows that the same mechanisms found in the digital circuit should also be present in the linear circuit. Relative frequency of occurrences may differ due to such differences as material resistivity, chip area, etc. In considering the foregoing factors, dc operational life tests were chosen for this program.

An analysis was made of each device at each stress level to determine the concentration of stress within the integrated circuit. These analyses are being formalized for presentation. The analysis of the MC-1519 was presented in the First Quarterly report. The analyses of the anticipated stress levels within the MC-1525 and MC-1530 are presented in this report. The analysis of the SN-526A will be formalized and presented in a subsequent report. As an adjunct in this effort in analysis, Motorola is investigating the development of circuit models which are compatible with computer analysis techniques. The results of this investigation will be presented in subsequent reports.

5.1 MC-1525 Life Test Analysis

The MC-1525 operational life test circuit is shown in Figure 5-1.

It can be shown that any unbalance between the currents of the differential transistors, Q_1 and Q_3 , has no effect as long as the sum of the currents remains constant. The circuit analysis may, therefore, be simplified by the use of a single equivalent stage in the collector of Q_2 . Figure 5-2 shows this equivalent circuit.

The circuit may be further simplified by the use of a Helmholtz-Thevenin equivalent circuit at the input to Q_2 with the parameters as shown in Figure 5-3.

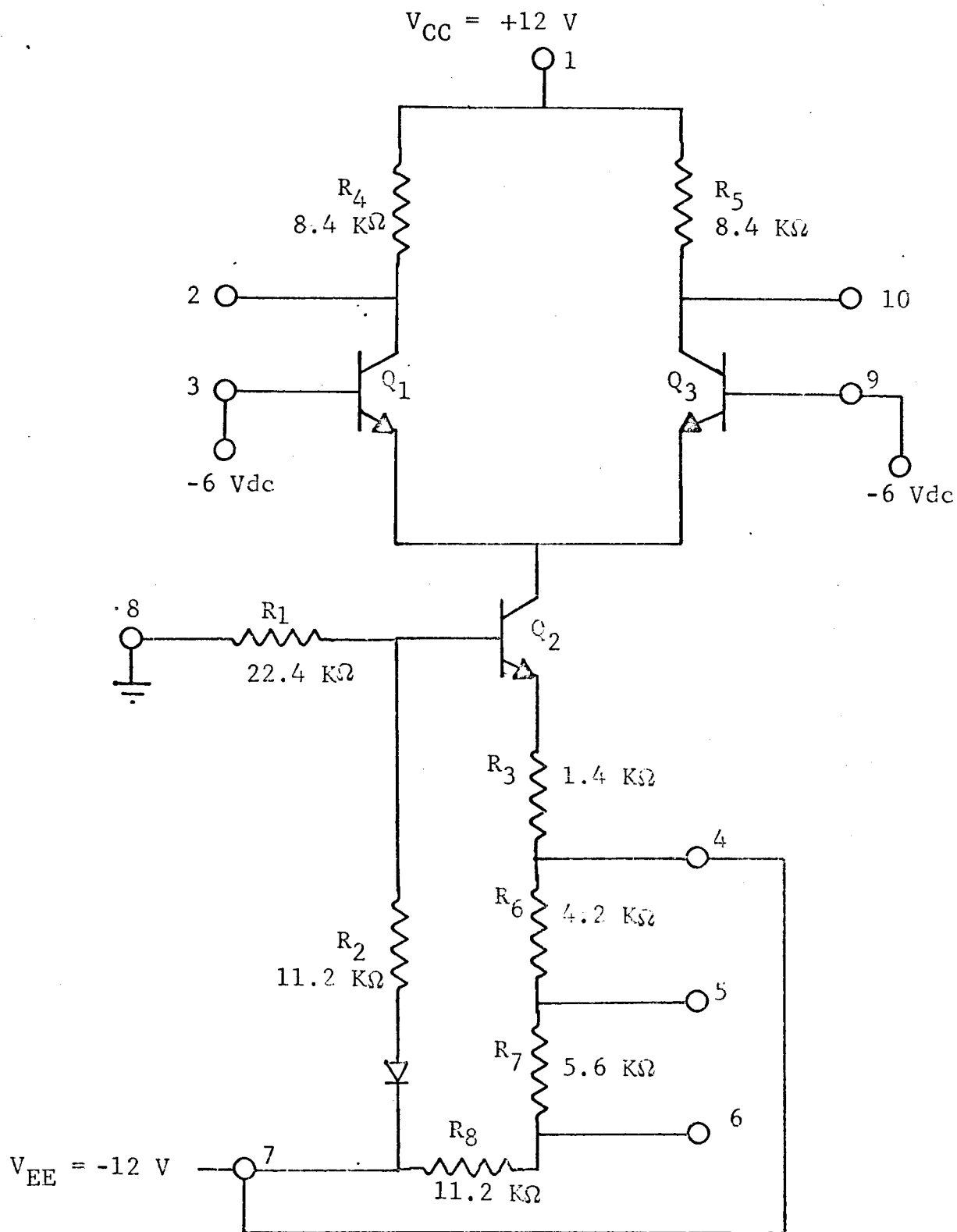


Figure 5-1. MC-1525 Operating Life Test Circuit

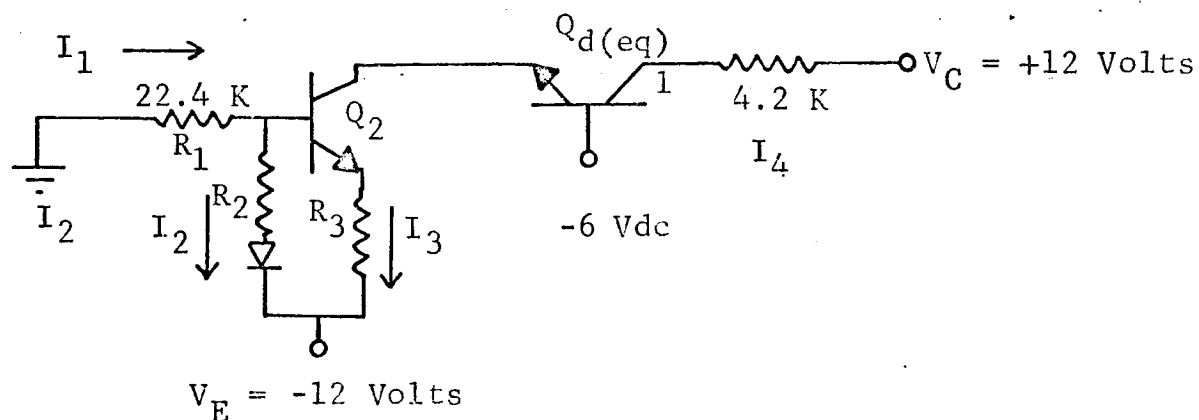


Figure 5-2. MC-1525 Equivalent Circuit

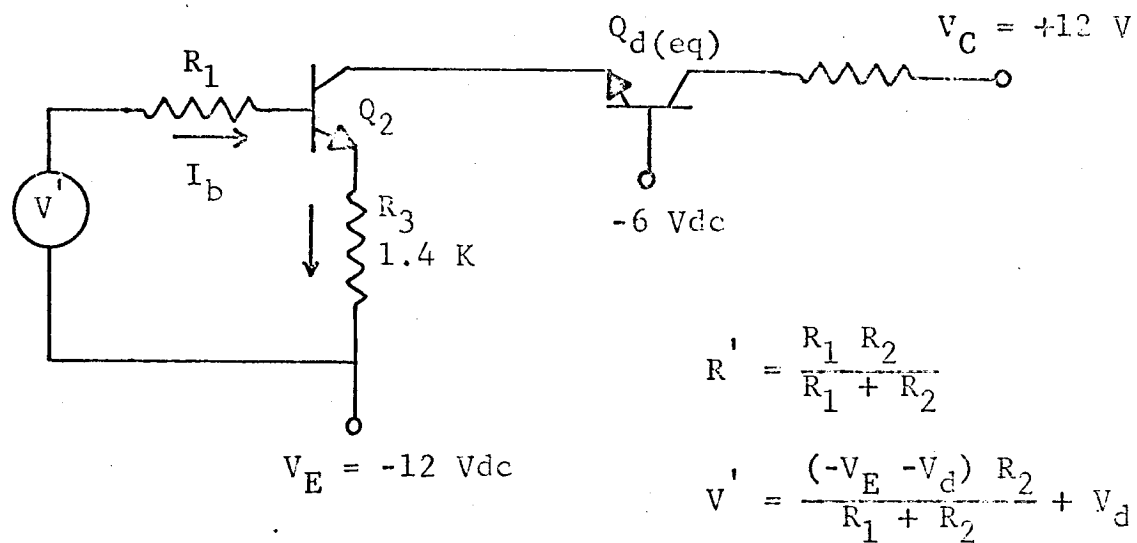


Figure 5-3. MC-1525 Equivalent Circuit Using Equivalent Voltage Source in Base of Q_2 .

Solving for the currents in Q_2 we have:

$$V' = I_b R' + (B + 1) I_b R_3 + V_{be}$$

$$V' = I_b [R' + (B + 1) R_3] + V_{be}$$

$$I_b = \frac{V' - V_{be}}{R' + (B + 1) R_3}$$

$$I_e = \frac{(B + 1) (V' - V_{be})}{R' + (B + 1) R_3}$$

$$I_c = I_e (Q_{eq}) = \frac{B (V' - V_{be})}{R' + (B + 1) R_3}$$

Evaluating the quantity $(V' - V_{be})$ assuming $V_d = V_{be} = 0.6$ Volts

$$V' = \frac{(-V_{EE} - V_d) R_2}{R_1 + R_2} + V_d$$

$$V' = \frac{[-(-12) - 0.6] 11.2 \times 10^3}{(11.2 + 22.4) 10^3} + 0.6$$

$$V' = \frac{11.4}{3} + 0.6 = 3.8 + 0.6 = 4.4 \text{ Volts}$$

$$V' - V_d = 3.8 \text{ Volts}$$

The equivalent source resistance, neglecting the dynamic resistance of the diode, is

$$R' = \frac{R_1 R_2}{R_1 + R_2} = \frac{11.2 \times 22.4}{11.2 + 22.4} \times 10^3 = \frac{22.4}{3} \text{ K } \Omega$$

$$R' = 7.47 \text{ K } \Omega$$

Assuming a β of to which corresponds to an $\alpha = 0.98$, then

$$I_b = \frac{3.8}{(7.47 + 51 \times 1.4) \times 10^3} = 48 \text{ uA}$$

$$V_{R_3} = (B + 1) I_b R_E = 51 \times 48 \times 10^{-6} \times 1.4 \times 10^3$$

$$V_{R_3} = 3.4 \text{ Volts}$$

$$V_{e(Q_2)} = V_{R_3} + V_{EE}$$

$$V_{E(Q_2)} = 3.4 + (-12) = -8.6 \text{ Volts}$$

$$V_{C(Q_2)} = -6.6 \text{ Volts}$$

$$V_{CE(Q_2)} = 2.0 \text{ Volts}$$

$$I_{C(Q_2)} = \beta I_b = 50 \times 48 = 2.4 \text{ mA}$$

$$V_{R_2} = V_{R_3} + V_{be} - V_d = 3.4 \text{ Volts}$$

$$I_2 = \frac{V_{R_2}}{R_2} = \frac{3.4}{11.2} \times 10^{-3} = .30 \text{ mA}$$

$$I_{E(Q_{eq})} = I_{C(Q_2)} = 2.4 \text{ mA}$$

$$V_{e(Q_{eq})} = V_{bb} - V_{be} = -6.6 \text{ Volts}$$

$$V_{C(Q_{eq})} = V_{cc} - \alpha I_e R_{(eq)}$$

$$V_{C(Q_{eq})} = 12 - 9.9 = 2.1 \text{ Volts}$$

and $V_{ce(Q_{eq})} = 2.1 - (-6.6) = 8.7 \text{ Volts}$

Calculating the total power

$$P_T = V_{CC} I_{CC} + V_{EE} I_{EE} + V_{BB} I_{bb(eq)}$$

$$P_T = 12 \times 2.35 \times 10^{-3} + (+12)(.3 + 2.45)10^{-3} + (-6)(+48)10^{-6}$$

$$P_T = 60.9 \text{ mW}$$

The power dissipation in each element in the device can now be evaluated

$$P_{R1} = (I_2 + I_b)^2 R_1 = (.348 \times 10^{-6})^2 \times 22.4 \times 10^3$$

$$P_{R1} = 2.7 \text{ mW}$$

$$P_{R2} = I_2^2 R_2 = (.3 \times 10^{-3})^2 \times 11.2 \times 10^3$$

$$P_{R2} = 1.0 \text{ mW}$$

$$P_R = I_3^2 R = [(B + 1) I_b]^2 R = [51 \times 48 \times 10^{-6}]^2 \times 1.4 \times 10^3$$

$$P_R = 8.4 \text{ mW}$$

Neglecting the $V_{be} I_b$ term

$$P_{Q2} = I_c V_{EE} = 2.0 \times 2.4 \times 10^{-3}$$

$$P_{Q2} = 4.8 \text{ mW}$$

Assuming $\alpha_{(Qeq)} = 1$

$$P_{R(eq)} = (I_{c(Qeq)})^2 R_{eq} = (2.35 \times 10^{-3})^2 \times 4.2 \times 10^3$$

$$P_{R(eq)} = 23.4 \text{ mW}$$

Assuming matched conditions on the differential transistors, Q_1 and Q_2 , this power may be assumed to divide equally, so that $1/2$ of the above power is dissipated in each resistor. The power dissipated in each resistor is then

$$P_{R_4} = P_{R_5} = 11.6 \text{ mW}$$

Using the value calculated for $V_{CE(Q_{eq})}$ and assuming a matched condition (0 offset) then

$$P_{Q1} = P_{Q3} = \frac{1}{2} (V_{CE} I_C)$$

$$P_{Q1} = P_{Q3} = \frac{1}{2} (8.7 \times 2.35)$$

$$P_{Q1} = P_{Q3} = 20.4 \text{ mW}$$

$$P_{D1} = 0.6 \times 0.3 = .18 \text{ mW}$$

Approximately 58 percent of the power is being dissipated in the resistor network and approximately 14 percent is dissipated in each of the input transistors, Q_1 and Q_3 , and 14 percent in the current source transistor, Q_2 .

5.2 MC-1530 Life Test Circuits

The following two sections present the analysis of the MC-1530 under the operating life test levels of 100 and 300 milliwatts. The 100 milliwatt test conditions are analyzed in some detail. The analysis of the 300 milliwatt test is based, in part, on the results of the 100 milliwatt analysis since the power dissipation increment is concentrated primarily in the output section.

5.2.1 MC-1530 100 Milliwatt Test Circuit

The life test circuit for the 100 milliwatt test is shown in Figure 5-4. In calculating the power dissipated in each circuit element, the external capacitance can be disregarded for its purpose is to suppress random oscillations that can occur if the circuit is not properly designed. Considering the input differential stage of the amplifier, we determine the voltages at different points in the circuit and thus estimate the power dissipated in the elements of that section of the device. If we assume that the input differential transistors are matched, the circuit may be redrawn as shown in Figure 5-4 for the bias conditions shown in Figure 5-5.

Assuming $\alpha = 1$ for both transistors, we may then calculate the voltage at base of Q_3 and use the voltage to calculate the current through R_2 , which is approximately equal to the collector current. Assuming $V_d = 0.7$ volts and $I_b \approx 0$.

$$V_{B-Q3} \approx \frac{(-6 + 2(0.7)R_5)}{(R_4 + R_5)} \approx -3.2 \text{ V} \quad (1)$$

then

$$I_{R_2} \approx \frac{V_{EE} - (V_{B-Q3} - 0.7)}{R_2} \approx 1.0 \text{ mA} \quad (2)$$

Then assuming that $I_{C-Q1} = I_{C-Q2} = 1/2 I_{C-Q3}$ ($\alpha = 1$) and resistors R_1 and R_3 are matched, the voltage at the collectors of Q_1 and Q_2 can be determined neglecting the base currents of Q_4 and Q_5 by the equation.

$$V_{C-Q1} \approx V_{C-Q2} \approx V_{CC} - \frac{R_3}{2R_2} \left[V_{EE} + 0.7 - \frac{(V_{EE} + 1.4) R_5}{R_4 + R_5} \right] \quad (3)$$

$$V_{C-Q2} \approx +2.2 \text{ Volts}$$

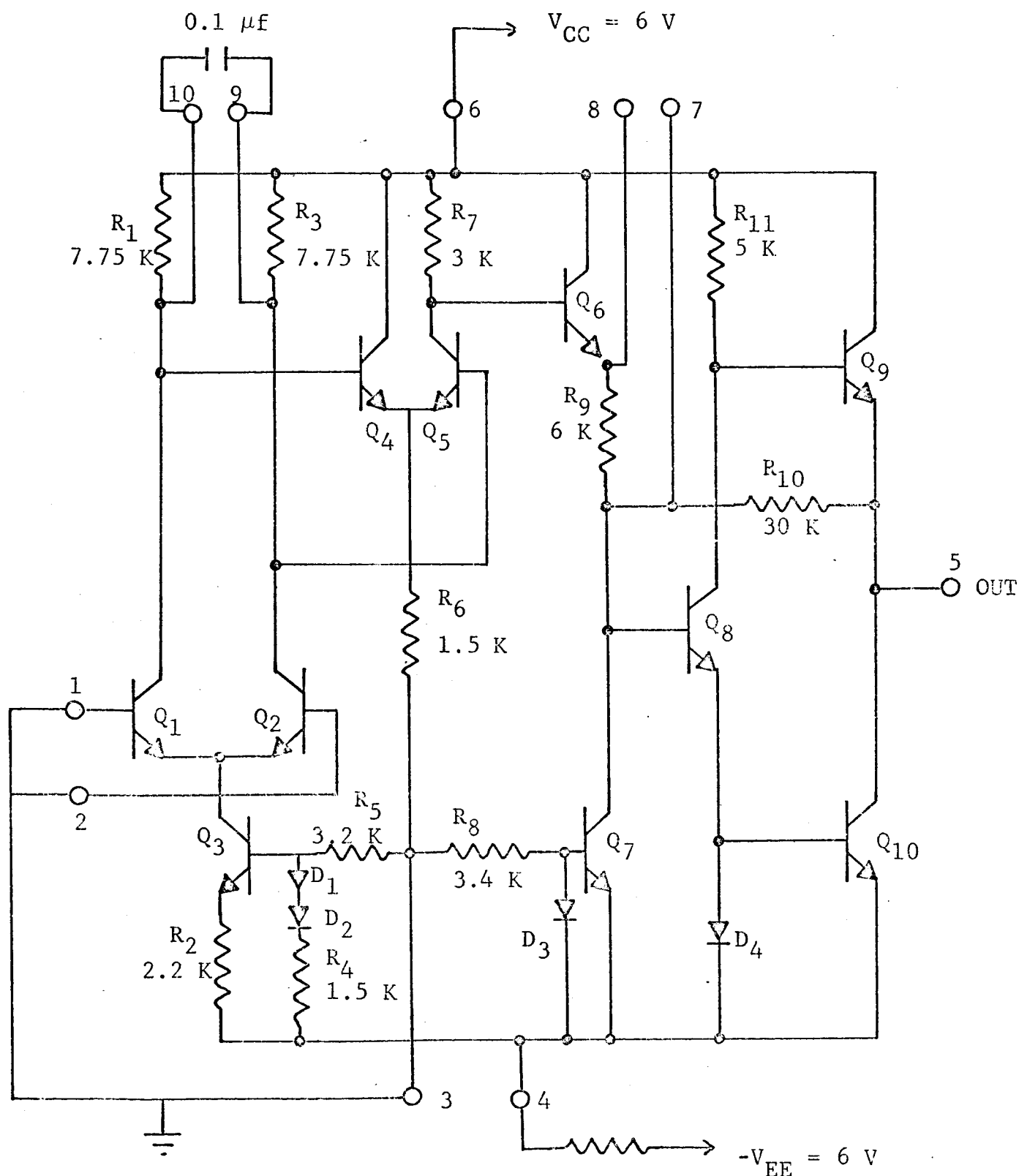


Figure 5-4. MC-1530 Operating Life Test Circuit

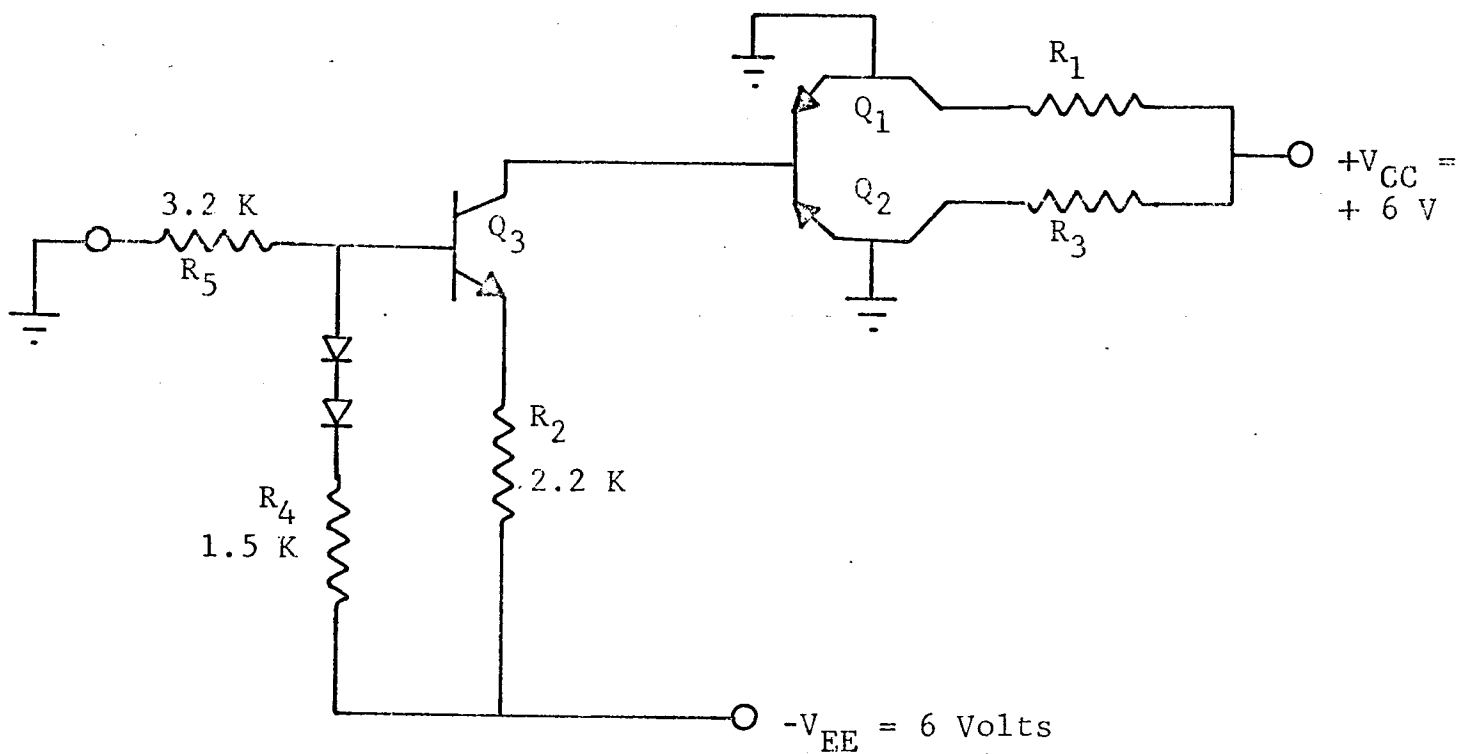


Figure 5-5. MC-1530 Input Differential Amplifier Section

This voltage also appears at the bases of Q_4 and Q_5 . The voltage at the emitter of these transistors is then:

$$V_{E-Q4} = V_{E-Q5} \approx V_{B-Q4} - 0.7 \quad (4)$$

$$V_{E-Q4} \approx 2.2 - 0.7 \approx 1.5 \text{ Volts}$$

and

$$I_{R_6} \approx \frac{1.5 \text{ Volts}}{1.5 \text{ K}} \approx 1 \text{ mA}$$

The voltage at the collector of Q_5 is then

$$V_{C-Q5} = V_{CC} - I_{C-Q5} R_7 \quad (5)$$

assuming that transistors Q_4 and Q_5 are matched and $\alpha \approx 1$, then

$$V_{C-Q5} = V_{CC} - I_C R_7 \quad (6)$$

$$V_{C-Q5} \approx 6 - 0.5 \times 3 \approx 4.5 \text{ volts}$$

and

$$V_{C-Q6} \approx 3.8 \text{ Vdc}$$

The meshes of the circuit consisting of R_8 , D_3 , and Q_7 may be analyzed in the following manner. The diode D_3 is formed as a transistor with the collector shorted to the base. The section is redrawn as shown in Figure 5-6.

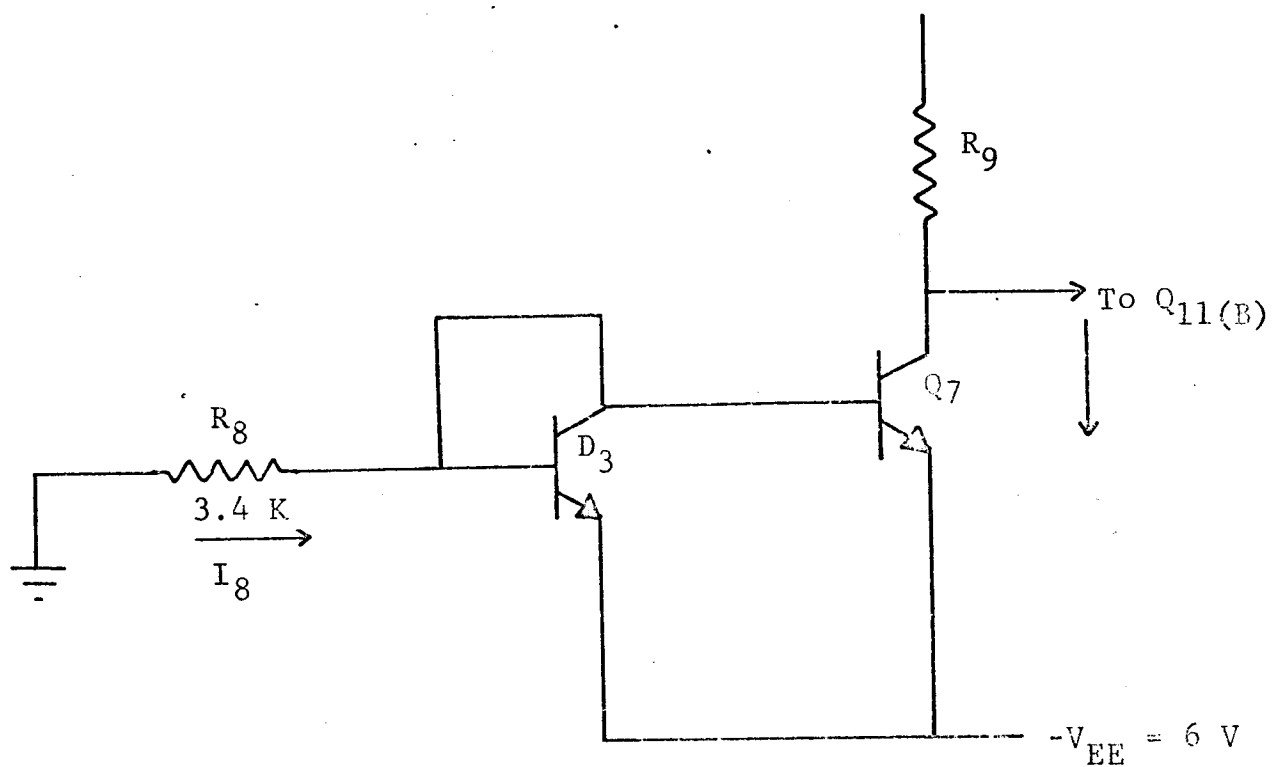


Figure 5-6. MC-1530 Level Shifter Section

The current through the transistor connected as D_3 will be

$$I_{R_8} = \frac{-V_{EE} - V_{BE}}{R_8} \quad (7)$$

$$I_{R_8} = \frac{6 - 0.7}{3.4 \text{ K}} = \frac{5.4}{3.4} = 1.58$$

If the transistors are identical then the current in the emitter of Q_7 will be equal to the current of the emitter of the diode connected transistor D_3 . Assuming further that $\alpha = 1$ then $I_{C-Q7} = I_{R_8}$ and the collector of Q_7 behaves as a collector of a common base stage and may be represented as a current source equal to 1.58 mA.

The level shifting and output stages may then be redrawn as shown in Figure 5-7. We can determine the voltage at the base of Q_8 as being two diode drops removed from $-V_{EE}$. Therefore:

$$I_{R_9} = \frac{V_{E-Q6} - V_{EE} - 1.4}{R_9} \quad (8)$$

$$I_{R_9} \approx \frac{3.8 + 6 - 1.4}{6 \times 10^3} \approx 1.4 \text{ mA}$$

Summing the currents at the base of Q_8 , neglecting the base current of Q_8 , we have

$$I_{R_{10}} + I_{R_9} = I_{Q7} \quad (9)$$

and

$$E_o = I_{R_{10}} R_{10} + V_{B-Q8} = I_{R_{10}} R_{10} + V_{EE} + 1.4 \text{ V} \quad (10)$$

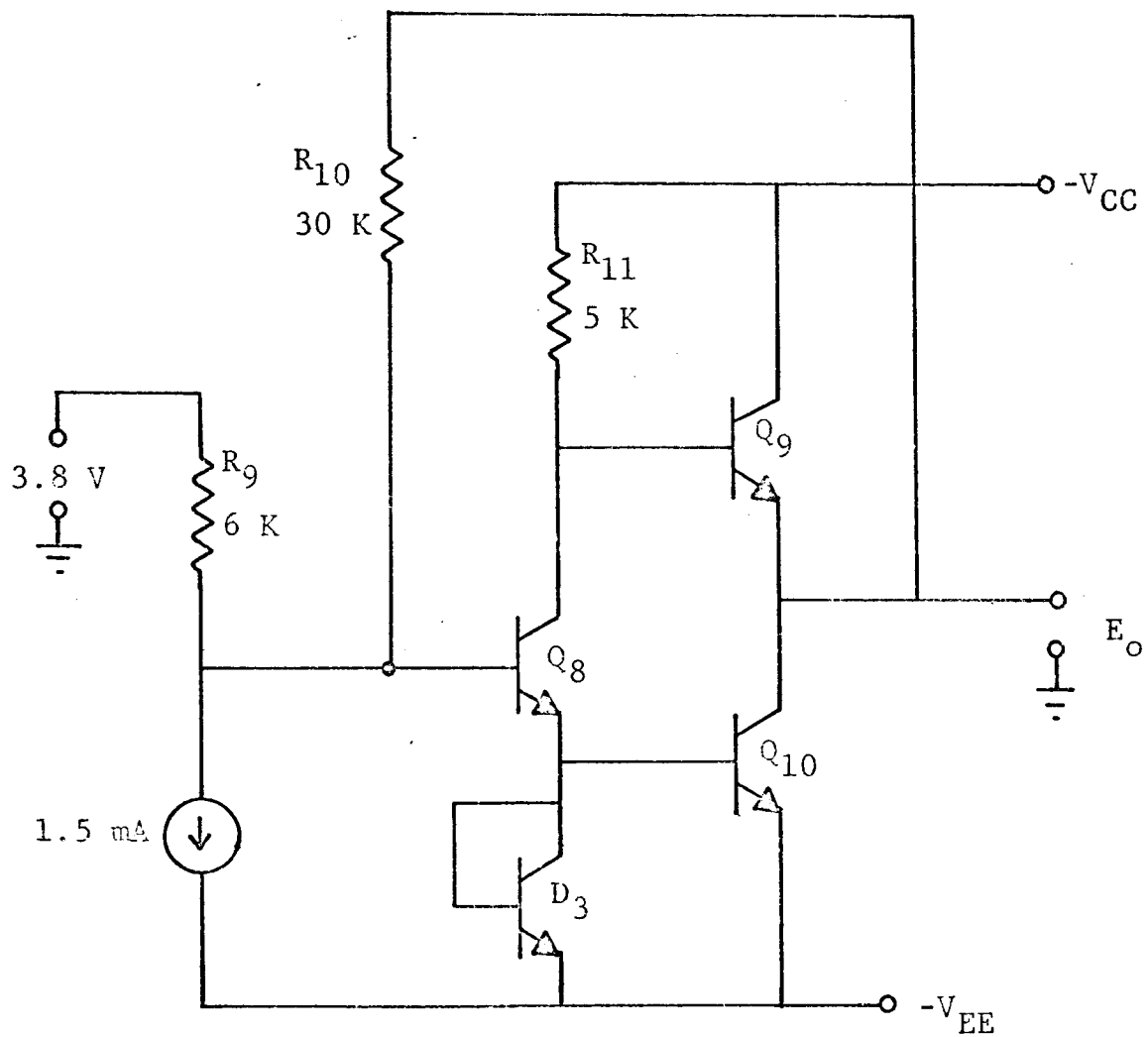


Figure 5-7. MC-1530 Level Shifter and Output Amplifier Equivalent Network

Substituting equations 7, 8, and 9 into equation 10 and simplifying we have:

$$E_o \approx -V_{EE} \left(\frac{R_{10}}{R_8} - \frac{R_{10}}{R_9} - 1 \right) - V_{E-Q6} \frac{R_{10}}{R_9} + 1.4 \left(\frac{R_{10}}{R_9} - \frac{R_{10}}{2R_8} + 1 \right) \quad (11)$$

$$E_o \approx 6 \left(\frac{30}{3.4} - \frac{30}{6} - 1 \right) - 3.8 \frac{30}{6} + 1.4 \left(\frac{30}{6} - \frac{30}{6.8} + 1 \right)$$

$$E_o \approx .16 \text{ volts}$$

This value is in error due to the approximation that $\alpha = 1$, as well as due to the round off of the value calculated for V_{E-Q6} . Were we to reflect this value of voltage back to the input, assuming typical gain, it would result in an offset of approximately -0.3 millivolt. This value is small considering the typical value of 1 millivolt given for this device.

Using the value of E_o calculated above then:

$$V_{C-Q6} = E_o + 0.7 = V_{C-Q6} \text{ volts}$$

$$I_{R_{11}} = \frac{V_{CC} - V_{C-Q6}}{R_{11}}$$

$$I_{R_{11}} = \frac{5.14}{5 \text{ K}} = 1.02 \text{ mA}$$

The combination of D_4 and Q_{10} is in the same form as D_3 and Q_7 except that the transistor Q_{10} is made up of three transistors connected in parallel, each of which is identical to the diode connected transistor. The emitter current of each, assuming identical characteristics, will be equal to the emitter current of D_4 and the total current which flows in Q_{10} will be approximately equal to 3 times the current which flows in D_4 , which is approximately 1.38 mA, as calculated above. The current in the output transistors will be:

$$I_{C-Q10} \approx I_{C-Q9} \approx 3 \times 1.02$$

$$I_{C-Q9} \approx 3.06 \text{ mA}$$

Using the values of the currents and voltages that have been calculated for typical component values, the power dissipation in each component is tabulated below for the 100 milliwatt level.

P_{R1}	1.9 mW	P_{Q1}	1.5 mW	P_{D1}	0.8
P_{R2}	2.2 mW	P_{Q2}	1.7 mW	P_{D2}	0.8
P_{R3}	1.9 mW	P_{Q3}	1.5 mW	P_{D3}	2.2
P_{R4}	1.4 mW	P_{Q4}	2.3 mW		
P_{R5}	3.1 mW	P_{Q5}	1.5 mW		
P_{R6}	1.5 mW	P_{Q6}	3.1 mW		
P_{R7}	0.8 mW	P_{Q7}	2.2 mW		
P_{R8}	8.6 mW	P_{Q8}	6.2 mW		
P_{R9}	11.8 mW	P_{Q9}	17.9 mW		
P_{R10}	0.8 mW	P_{Q10}	18.9 mW		
P_{R11}	5.2 mW				
Total $P_R \approx 39.2 \text{ mW}$		P Transistor $\approx 56.8 \text{ mW}$		$P_d \approx 3.8 \text{ mW}$	

Total power = 99.8 milliwatts

5.2.2 MC-1530 - 300 Milliwatt Life Test

The test circuit used in the 300 milliwatt test is a modification of the 100 milliwatt test circuit. This modification consists of connecting a variable resistance between pin 7 and 8, which effectively varies the resistance of R_9 . It has been empirically determined that the value of resistance used to produce 300 milliwatts does not cause significant loading on the input differential stage. The operation of Q_4 and Q_5 , the second differential pair, is also not appreciably affected. We can, therefore, represent the circuit operating at the 300 milliwatt level with the network shown in Figure 5-8. The resistor R_k represents the parallel combination of R_9 and the external rheostat.

From Figure 5-8 it is seen that the total power supplied by V_{CC} and V_{EE} must equal the sum of the power in the box representing the differential amplifier and the Q_7 current source, and that ΔI_{CC} and ΔI_{EE} differ by 0.5 mA. The power which must be dissipated in the output section is then:

$$300 - 33 = 267 \text{ mW}$$

$$\text{by inspection } \Delta I_{EE} + 0.5 = \Delta I_{CC}$$

$$\text{and } \Delta I_{EE} = \frac{267 - 3.0}{12} = 22 \text{ mA}$$

The power dissipated in the shunt resistor must be considered. It was experimentally determined that the 300 milliwatts could be achieved with a nominal shunt resistance of 570 ohms and a current drain of approximately 30 milliamperes would yield the proper power dissipation. At these conditions the total power supplied per device is 360 milliwatts of which approximately 60 milliwatts is dissipated in the external resistor. The average

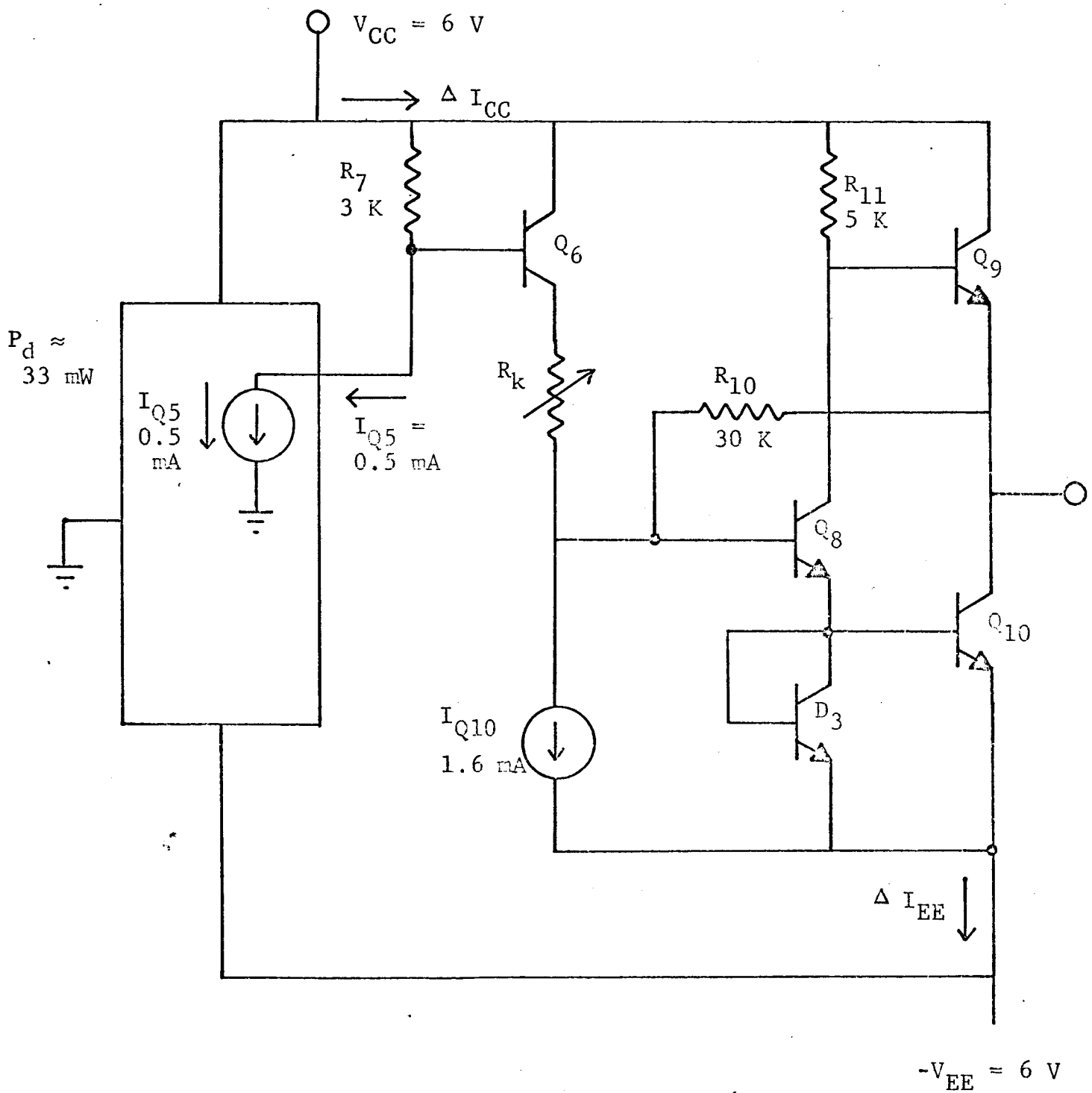


Figure 5-8. MC-1530 - 300 Milliwatt Life Test Equivalent Circuit.

voltage across R_k was determined to be 5.7 volts. The value R_k can be determined by

$$R_k = \frac{(R_{sh})(R_9)}{R_{sh} + R_9}$$

$$R_k = \frac{570 \times 6000}{6570} = 520 \text{ ohms}$$

adjusting ΔI_{EE} for the power in the shunt resistor, we have

$$\Delta I_{EE} = 22 + \frac{60}{12}$$

$$\Delta I_{EE} = 27 \text{ mA}$$

I_{Rk} can be determined by

$$I_{Rk} = \frac{V_{Rk}}{R_k}$$

$$I_{Rk} = \frac{5.7}{5.2} = 11.0 \text{ mA}$$

and

$$I_{b-Q8} = I_{Rk} - I_{Q7} - I_{R10}$$

neglecting I_{R10} which will be quite small:

$$I_{B-Q8} \approx 11.0 - 1.6 \approx 9.4 \text{ mA}$$

since the collector load resistance, R_{11} , is equal to 5 K, Q_8 will be saturated as, for that matter, will be Q_{10} . The distribution of current between the output loop (Q_9 and Q_{10}) and the driver loop (R_{11} , Q_8 , and D_3) will be determined by the difference between V_{SAT} of transistors Q_8 and Q_{10} and the difference between V_{BE} , Q_9 , and V_{D3} . This renders the circuit indeterminate to piecewise linear analysis.

The emitter current in Q_8 is equal to the sum of the base and collector currents. The collector current in Q_8 can be determined by

$$I_{C-Q8} = \frac{V_{CC} - V_{EE} - (V_{D3} - V_{CESAT})}{R_{11}}$$

The offset voltage for this type of transistor will be on the order 0.1 volts and the value of R_{sc} will be approximately 75 ohms, at a level of 2 milliamperes. The value of V_{SAT} will be approximately 0.25 volts and we may assume that $V_{D3} = 0.8$ volts. Therefore

$$I_{C-Q8} \approx \frac{12 - 1.05}{5 \text{ K}} \approx 2.2 \text{ mA}$$

and

$$I_{E-Q8} \approx 11.6 \text{ mA}$$

Regardless of the division of currents between D_3 and Q_{10} , the sum of the currents at the emitter node of Q_{10} must be 27 mA; therefore

$$I_{C-Q10} = 27 - 11.6 - 1.6 = 13.8 \text{ mA}$$

The voltage at the emitter of Q_6 was found to average 1.2 volts; therefore:

$$V_{CE-Q6} = 6 - 1.2 = 4.8 \text{ volts}$$

and assuming $V_{BE} \approx 0.7$ volts

$$V_{R7} = 4.1 \text{ volts}$$

In the foregoing analysis, the current in R_{10} has been ignored as has the base current in Q_9 .

The power in the critical elements may now be evaluated. Since Q_{10} is saturated, most of the power in the output loop will appear at Q_9 . Power in the highly stressed components are

$$P_{Q9} \approx 13.8 \times 12.0 = 166 \text{ mW}$$

$$P_{Q6} \approx 4.8 \times 9.4 = 45 \text{ mW}$$

$$P_{R11} \approx 11 \times 2.2 = 24 \text{ mW}$$

The power dissipated in Q_8 , Q_{10} , and D_3 will be approximately 15 milliwatts and the power in R_7 , R_9 , and the current generator, I_{Q10} , totals 13.2 milliwatts.

SECTION VI

6.0 SURVEY OF LITERATURE

This section of the quarterly report describes the survey of existing literature included as part of the program to determine the failure modes and mechanisms of integrated circuits. The selection of source documents is described. Conduct of the survey is discussed. Failure mechanisms are listed and described.

6.1 Source Documents

Two hundred and seventeen documents or articles have been selected for review and study. A list is attached as an Appendix. Included in the items selected are previous studies and tests, publications, articles in professional journals, and presentations made at the various symposia conducted in the reliability engineering field. Of the documents and articles selected, 169 have been received and were studied. Those containing the required information and data were used as references in the listing of failure mechanisms. The 48 other documents will be similarly studied when received. Results of their study will be included in the final report of the program. The major source of the information and data assembled to date has been the Proceedings of the Physics of Failure in Electronics Symposia sponsored annually by Rome Air Development Center in conjunction with the IIT Research Institute and, this year, the Battelle Memorial Institute. Additional programs from which significant masses of information were gleaned were the many studies and tests conducted for Rome Air Development Center in its reliability physics program since 1961 and the Component Quality Assurance Program (CQAP) conducted by Autonetics to improve the reliability of the Minuteman Missile System.

6.2 Discussion

In studying the source materials, it was noted that wide differences in interpretation and usage of the terms "failure mode" and "failure mechanism" exist in the field of semiconductor technology. They occur not only among the various organizations but also within an organization. Documents defining these terms have later included tabulations which used such terms as "failure indicator", "failure cause", "basic physical phenomenon", etc., in lieu of the defined terminology. To avoid ambiguity and misunderstanding, the term "failure mechanism" is the only term used in this report and is defined as: The fundamental physical mechanisms that are responsible for the change causing the observed failure. These mechanisms are considered to be independent causes of failure.

Study of the source materials could not establish the relative rates of incidence of the various failure mechanisms because quantitative data were furnished in only a few reports of test. However, a review of the Autonetics studies and two recent studies (references 105 and 135) establishes that the prevalent causes of failure are imperfections of bonds, interconnects, and passivation and surface instabilities resulting from surface contamination, to include inversion channelling.

Many of the source documents did not identify specific failure mechanisms as being responsible for the device failures reported therein. They have been listed in the Appendix for information but are not used as references in the following paragraph.

6.3 Failure Mechanisms

The failure mechanisms are listed below in the order: bonds, interconnects, passivation, surface contamination, bulk

defects, and other miscellaneous failure mechanisms in the order in which they may be introduced during the fabrication process.

6.3.1 Failure Mechanisms Associated With Bonds

INTERMETALLIC COMPOUND FORMATION -

Open and intermittent bonds were experienced in devices having gold-aluminum metallization when stored at 200° and 300°C. Initially, the failure mechanism was identified as gold diffusing into aluminum to form AuAl₂ (purple plague). Subsequently, the failure mechanism was identified as a ternary compound of Au-Al-Si (black death). More recently, the failure mechanism has been identified to be due to the formation of gold-rich Au-Al compounds in the order AuAl, Au₂Al, Au₅Al₂, Au₄Al and gold (solid solution of aluminum in gold). Although not all authorities agree as to the specific failure mechanism involved, it is established that gold diffuses into aluminum, that silicon present near the Au-Al interface apparently acts as a catalyst in the diffusion, and that it proceeds more rapidly at higher temperatures. The effects of this failure mechanism have been reduced by utilizing all-aluminum metallization or by using aluminum leads within the package to form the Au-Al bond on the TO-5 post or on the flat-package bonding pad. (References: 1, 6, 14, 18, 19, 21, 36, 51, 54, 55, 61, 66, 69, 72, 74, 77, 83, 104, 105, 113, 119, 120, 124, 129, 136, 139, 148, 149, 155, 172, 174, 182, 185.)

OPEN BOND - OVERBONDING -

Open, intermittent, high-resistance, and shorted circuits were found to have been caused by overbonding. The open, intermittent, and high-resistance circuits normally result from the application of excess pressure by the bonding tool on the lead in the wire bonding process, either severing the lead completely or

crimping it sufficiently to reduce materially its effective cross-sectional area for current transfer. The shorted circuits normally result from the application of excess temperature which splatters lead material on the surface of the device. Records of this failure mechanism usually include the location at which the defective bond occurs; e.g., on the pad, at post, etc. (References: 5, 18, 19, 21, 58, 61, 66, 69, 72, 75, 77, 83, 89, 105, 119, 124, 125, 134, 135, 136, 139, 143, 151, 155, 185.)

OPEN BOND - UNDERBONDING -

Both open and intermittent bonds were found to be caused by underbonding. This results from insufficient pressure and/or temperature in performing the bonding operation. Reports for this failure mechanism usually include the description of the type of underbonding experienced and the location at which it occurs; e.g., separation of bond from pad, insufficient contact area, voids or cracks in bond, separation of lead from terminal, etc. (References: 5, 14, 19, 21, 39, 40, 51, 55, 61, 64, 66, 69, 72, 77, 83, 89, 104, 105, 119, 120, 124, 125, 134, 135, 136, 139, 143, 149, 155, 185.)

IMPROPER BOND LOCATION -

Some intermittent and shorted circuits were found to have been caused by bonds formed too close to the edge of the interconnect or the die. In the former case, the failure mechanism was usually identified as one of the failure mechanisms of proper passivation; e.g., pinholes in oxide, scratches in oxide, etc. In the latter case, the bond was found to have shorted to the substrate material either directly or by a shunt across the oxide surface. (References: 9, 21, 49, 64, 105, 125, 179.)

6.3.2 Failure Mechanisms Associated With Interconnects

IMPROPER INTERCONNECT -

Specific failure mechanisms listed under the general heading of improper interconnect are: poor adhesion of the metal, improper thickness of the metal, improper width of the metal, and cracks and scratches in the metal. The first three are normally caused by improper diffusion. The latter is normally caused by carelessness in processing. The effect of all of these failure mechanisms is to reduce the effective cross-sectional area for current transfer. When the current density at any of these constrictions increases to a value at which heat energy is produced faster than the substrate can carry it away, hot spots are experienced and thermal runaway may occur. (References: 7, 14, 19, 21, 51, 64, 66, 69, 83, 104, 105, 119, 130, 134, 137, 139, 154, 179.)

IMPROPER METALLIZATION -

The specific failure mechanisms listed under the general heading of improper metallization are: decomposition of the metal, corrosion of the metal, and oxidation of the metal. Freshly deposited metal may contain an abnormally high concentration of lattice defects. When these lattice vacancies or interstitial atoms gradually disappear under the annealing conditions of later processing steps or use, a change in the metallization occurs. In addition, impurities and contaminants, particularly moisture, entrapped within the package may react chemically with the metal. The effect of either condition is a change in the sheet resistivity of the metal film, thus causing localized heating at constrictions. When heat energy is produced faster than the substrate can carry it away, hot spots are experienced and thermal runaway may occur. (References: 5, 6, 9, 18, 19, 21, 64, 66, 88, 91, 105, 124, 129, 135, 137, 139, 149, 155.)

METAL DIFFUSION INTO SILICON -

Circuit failures were experienced when the gold or aluminum metallization diffused into junction regions, isolation regions, or the die. Gold has been shown to migrate rapidly across silicon. Aluminum has been shown to migrate from the areas of metallization, particularly at the edges and at steps in the oxide, when devices were stored at 150° to 350°C for periods ranging from 2,500 to 11,000 hours. Aluminum has been shown to react with the oxide passivation to form an aluminum oxide and silicon at temperatures ranging from 250° to 560°C. The effect of this failure mechanism can be reduced by proper passivation of devices since the metal diffuses fastest in partially passivated or unpassivated areas through regions abounding in pinholes, scratches, etc. (References: 5, 7, 18, 21, 26, 29, 53, 61, 72, 76, 95, 113, 135, 148, 154, 175, 179.)

6.3.3 Failure Mechanisms Associated With Passivation

Specific failure mechanisms listed under the general heading of improper passivation are: pinholes in oxide, cracks in oxide, scratches in oxide, feathering of oxide, flaking of oxide, undercutting of oxide, and insufficient thickness of oxide, to include unpassivated areas. The partially passivated or unpassivated areas cause failure by providing a shunt for current flow or by permitting impurities and contaminants to diffuse into the surface of the die. The failure mechanisms of improper passivation are related to the other failure mechanisms which identify partially passivated or unpassivated areas. (References: 7, 8, 14, 19, 21, 34, 58, 60, 66, 67, 83, 88, 101, 104, 105, 108, 114, 116, 119, 120, 124, 126, 134, 136, 138, 139, 146, 151, 154, 155, 158, 179.)

6.3.4 Failure Mechanisms Associated With Surface Contamination

INVERSION CHANNELLING -

Inversion channelling has been the subject of many articles in professional journals and presentations at the symposia. It occurs when a bias voltage applied across a PN junction causes mobile impurity ions (on the surface of the passivation, within the passivation, or at the interface between the passivation and the surface) to move to create a concentration of charges over the semiconductor material adjacent to the junction. This charge concentration causes a concentration of carriers of opposite polarity in the surface of the silicon adjacent to the junction and when great enough, will invert p-type material to n-type material (or n-type material to p-type material). It has been shown that this condition is temperature-dependent (i.e., high ambient or junction temperature accelerates the failure mechanism) and that the inversion of only a few monolayers at the semiconductor surface is necessary to create a channel of electrical significance. This failure mechanism is manifested by an increase in leakage current and, in some cases, a decrease in gain at low collector currents. It is reversible by baking the devices at 200°C for 3-5 hours with no bias voltage applied. (References: 1, 2, 3, 5, 11, 21, 22, 23, 24, 25, 32, 49, 57, 58, 60, 76, 88, 89, 90, 91, 92, 96, 100, 101, 109, 113, 119, 128, 136, 138, 139, 157, 159, 161, 172, 175.)

SURFACE CONTAMINATION -

Device failures were found to be caused by the presence of organic materials left on the die surface during processing of the device in fabrication. These materials caused device failure by providing a resistive short between circuit elements or by

reacting chemically with the device materials. (References: 2, 8, 9, 19, 20, 21, 24, 28, 29, 39, 47, 49, 60, 61, 66, 67, 72, 88, 91, 105, 109, 112, 116, 117, 120, 124, 128, 133, 134, 135, 136, 139, 143, 147, 154, 155, 161, 163, 175, 179.)

CRACKS AND SCRATCHES IN DIE -

Cracks in silicon die were found to be caused primarily by overpressure applied during the die-to-header bonding operation or by mechanical stress induced in the dice by changing thermal conditions or shock and vibration in cases where the die was not thoroughly attached to the header throughout the interface. Scratches in dice were found to result during processing. Cracks or scratches occurring before passivation may result in failures from other failure mechanisms, such as metal diffusion into silicon, pinholes in oxide, etc. Those occurring after passivation provide shunts for current flow or partially passivated or unpassivated paths by which impurities and contaminants within the package diffuse into the die, causing eventual failure of the die. (References: 5, 18, 20, 21, 39, 49, 54, 58, 64, 66, 69, 80, 82, 89, 105, 119, 124, 134, 135, 139, 143, 179, 188.)

ETCH PITS -

Etch pits were found to cause failures because they provided areas contributing to improper passivation of the surface and eventual diffusion into the die of the impurities and contaminants present within the package. (References: 20, 34, 50, 64, 76, 80, 82, 88, 151, 175, 188.)

FAULTY SEAL -

Device failures were found to be caused by faulty seals which permitted contaminants, particularly moisture, to penetrate the package and react chemically with the device materials. The

specific failure mechanisms listed under the general heading of faulty seal are: faulty cap-to-case seal, faulty preform-to-case seal, broken insulation around terminal, and faulty insulator-to-case seal. The faulty seals were found to be caused by poor wetting of the elements of the seal during assembly or breaking of insulation due to mechanical stresses created in the interface by differences in the thermal expansions of the elements of the seal. (References: 15, 21, 22, 49, 64, 69, 70, 83, 114, 134, 135, 136, 139, 143, 179.)

FOREIGN MATERIAL INSIDE PACKAGE -

The two predominant types of device failure experienced from foreign material inside the package were shorts caused by conducting material and mechanical damage caused by nonconducting materials during shock and vibration testing. (References: 2, 21, 49, 61, 64, 66, 69, 80, 88, 105, 117, 119, 120, 124, 125, 126, 129, 130, 133, 134, 136, 139, 179.)

6.3.5 Failure Mechanisms Associated With Bulk Defects

EXPITAXIAL DEFECTS -

Edge dislocations, isolated dislocations, twin boundaries, stacking faults and "stair-rod" dislocations associated with stacking faults were found to exist in the silicon wafer. There is little evidence that these defects, in themselves, have a deleterious effect on the operation of semiconductor devices. However, it is established that such lattice imperfections yield nonuniform doping and provide nucleation centers for impurity precipitation. "Stair-rod" dislocations have been established as the most serious of these types of defects. (References: 5, 20, 21, 26, 28, 33, 34, 49, 59, 67, 76, 80, 81, 82, 83, 119, 126, 133, 138, 151, 158, 163, 188.)

BULK DEFECTS -

Relatively few failures were found to have been caused by bulk defects. Devices made from wafers having bulk defects which are inherent in the wafer or are introduced during processing are normally rejected during production line electrical tests. The failure mechanism bulk defects, as used in this survey categorizes those failures for which another failure mechanism cannot be found. As an example, if a transistor were to degrade under the temperature, voltage, and current conditions of its use and all other possible failure mechanisms (e.g., diffusion of metal into silicon, surface contamination, pinholes in oxide, etc.) were eliminated, bulk defects might have been the failure mechanism postulated as responsible for the failure. Included within this failure mechanism are failure modes caused by current concentration centers, unstable or improper resistors, and faulty capacitors, diodes, and transistors. However, the references listed below also include failures reported as due to this mechanism for which failure analyses did not continue until a specific failure mechanism was identified. (Reference: 11, 15, 19, 20, 21, 30, 36, 49, 58, 60, 61, 64, 68, 69, 70, 89, 96, 105, 109, 112, 113, 117, 120, 125, 133, 136, 139, 143, 147, 155, 161, 166, 175, 179.)

6.3.6 Miscellaneous Failure Mechanisms

IMPROPER MASKING OR ETCHING -

Relatively few failures were found to have been caused by improper masking or etching. Devices made from wafers having imperfections due to these processing errors are normally rejected during production line electrical tests. In those cases where the imperfections are not detected by electrical tests, subsequent failure analysis defines more specifically the failure mechanism responsible for failure (e.g., undercutting of oxide, improper thickness of oxide, etc.). (References: 19, 21, 61, 64, 66, 69, 83, 88, 105, 120, 126, 138, 139, 155, 179.)

MISORIENTATION OF DIE -

Relatively few failures were found to have been caused by the misorientation of the die within the package, improper design layout, or improper marking of the pins of the device. In most cases, the devices having this failure mechanism are rejected during production line electrical tests or the failure mechanism is identified as one of the other failure mechanisms, e.g., lead routing, sagging leads, etc. (References: 21, 66.)

VOID UNDER DIE AND LOOSE DIE -

Hot spots and thermal runaway were found frequently to be caused by voids under dice and loose dice because the heats generated in use were not dissipated through the die-to-header bond to the package. This failure mechanism results from poor wetting of the die and/or the header during assembly. (References: 9, 21, 29, 30, 39, 49, 52, 53, 54, 55, 58, 66, 89, 91, 112, 119, 134, 135, 136, 139, 143.)

IMPROPER LEADS -

Specific failure mechanisms listed under the general heading of improper leads are: improper lead routing, sagging leads, excessive lead length, insufficient lead length, and broken leads. Intermittent and shorted circuits were found to have been caused by the first three failure mechanisms when leads touched other leads, the die, the package lid, or the metal interconnect. Open and intermittent circuits were found to have been caused by leads breaking from excess tension (too short) and leads which had been damaged or broken during processing in fabrication. (References: 9, 19, 21, 66, 69, 70, 89, 105, 124, 125, 136, 139, 175, 179.)

CRACKED DIE -

Cracked dice were experienced in devices subjected to repeated temperature cycles. This failure mechanism was determined to be caused by mechanical stresses created in the die by differences in the thermal expansions of the die, the eutectic, and the header. It was eliminated by utilizing materials having more compatible coefficients of thermal expansion. (SIC) (References: 5, 20, 31, 49, 53, 54, 58, 134.)

EXTERNAL SURFACE CONTAMINATION -

External surface contamination was found to have caused electrically "good" dice to be classified as failures. Contamination on the package provided external leakage paths between terminals or between a terminal and the package. These contaminants may be present because of improper cleaning or handling or because of the use of improper materials. (References: 5, 21, 49.)

APPENDIX

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